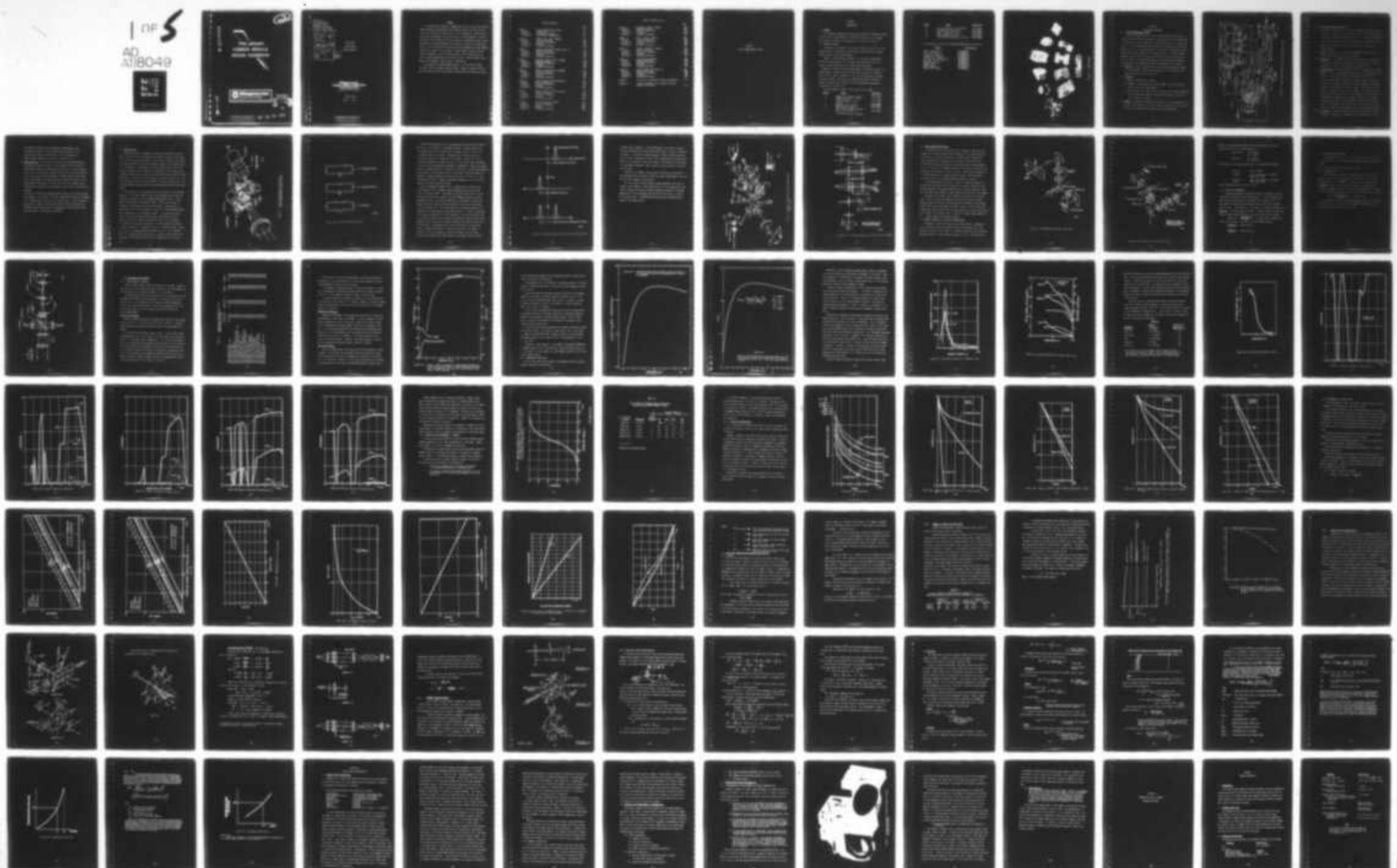
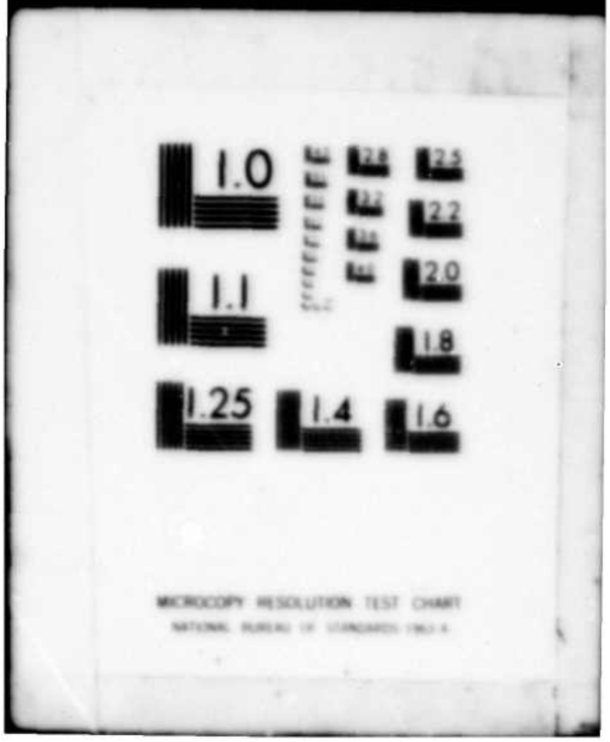
AD-A118 049 MAGNAVOX GOVERNMENT AND INDUSTRIAL ELECTRONICS CO MA--ETC F/G 9/5
PRELIMINARY COMMON MODULE DESIGN HANDBOOK.(U)
APR 76 DAAG53-75-C-0178
UNCLASSIFIED GSDR-900 NL

1 OF 5
AD
A118049



18049


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

AD A118049

PRELIMINARY COMMON MODULE DESIGN HANDBOOK

Magnavox

ELECTRO-OPTICAL SYSTEMS

82 08 09 104

Prepared for:
U.S. Army Mobility
Equipment Research &
Development Center
Night Vision Laboratory
Ft. Belvoir, Va. 22060
Contract: DAAG53-75-C-0178

PRELIMINARY COMMON MODULE DESIGNER HANDBOOK

Magnavox
GOVERNMENT & INDUSTRIAL ELECTRONICS COMPANY
ADVANCED PRODUCTS DIVISION
ELECTRO-OPTICAL SYSTEMS

GSDR No. 900

April 2, 1976

FORWARD

This Common Module Designer's Handbook was written in order that users of Common Modules and Common Module Thermal Imaging Systems or FLIR's are provided with information on the function, theory of operation, interface problem., and the maintenance, testing and care of the Common Modules. The U.S. Army Night Vision Laboratory (NVL) has successfully developed a number of Common Modules which when assembled into a system can be used for various applications. The individual FLIR functions have been seperated and unique modules, that have the flexibility to be used in Thermal Imaging Systems of various levels of complexity, satisfy the large majority of Army applications, as well as numerous applications of the other services. Special system unique modules can be added to satisfy specific requirements.

The purpose of the Common Module program is to significantly reduce the cost of real time Thermal Imaging Systems. Quantity production of common units which satisfy a large number of applications will achieve this goal.

TABLE OF CONTENTS

		Page
CHAPTER 1	TYPICAL COMMON MODULE SYSTEM	-1-
SECTION I	INTRODUCTION	-2-
SECTION II	FUNCTIONAL DESCRIPTION	-5-
SECTION III	SYSTEM DESIGN CONSIDERATION	-81-
CHAPTER 2	PREAMPLIFIER, VIDEO, INFRARED	-89-
SECTION I	GENERAL DESCRIPTION	-90-
SECTION II	FUNCTIONAL DESCRIPTION	-92-
SECTION III	INTERFACE	-97-
SECTION IV	ALIGNMENT/MAINTENANCE	-105-
CHAPTER 3	POSTAMPLIFIER/CONTROL DRIVER, VIDEO, IR	-113-
SECTION I	GENERAL DESCRIPTION	-114-
SECTION II	FUNCTIONAL DESCRIPTION	-116-
SECTION III	INTERFACE	-121-
SECTION IV	ALIGNMENT/MAINTENANCE	-129-
CHAPTER 4	AUXILIARY CONTROL, VIDEO, INFRARED	-138-
SECTION I	GENERAL DESCRIPTION	-139-
SECTION II	FUNCTIONAL DESCRIPTION	-141-
SECTION III	INTERFACE	-150-
SECTION IV	ALIGNMENT/MAINTENANCE	-157-
CHAPTER 5	REGULATOR, DETECTOR BIAS, INFRARED	-166-
SECTION I	GENERAL DESCRIPTION	-167-
SECTION II	FUNCTIONAL DESCRIPTION	-169-
SECTION III	INTERFACE	-173-
SECTION IV	ALIGNMENT/MAINTENANCE	-178-
CHAPTER 6	DC/AC INVERTER P/O COOLER/INVERTER	-184-
SECTION I	GENERAL DESCRIPTION	-185-
SECTION II	FUNCTIONAL DESCRIPTION	-187-
SECTION III	INTERFACE	-194-
SECTION IV	ALIGNMENT/MAINTENANCE	-200-
CHAPTER 7	MODULAR COOLER P/O COOLER/INVERTER	-207-
SECTION I	GENERAL DESCRIPTION	-208-
SECTION II	FUNCTIONAL DESCRIPTION	-210-
SECTION III	INTERFACE	-212-
SECTION IV	ALIGNMENT/MAINTENANCE	-221-
CHAPTER 8	SCAN AND INTERLACE INFRARED	-230-
SECTION I	GENERAL DESCRIPTION	-231-
SECTION II	FUNCTIONAL DESCRIPTION	-234-
SECTION III	INTERFACE	-242-
SECTION IV	ALIGNMENT/MAINTENANCE	-254-

TABLE OF CONTENTS (Cont.)

		Page
CHAPTER 9	COLLIMATOR, VISUAL, INFRARED	-266-
SECTION I	GENERAL DESCRIPTION	-267-
SECTION II	FUNCTIONAL DESCRIPTION	-270-
SECTION III	INTERFACE	-272-
SECTION IV	ALIGNMENT/MAINTENANCE	-281-
CHAPTER 10	IMAGER, OPTICAL, INFRARED	-290-
SECTION I	GENERAL DESCRIPTION	-291-
SECTION II	FUNCTIONAL DESCRIPTION	-294-
SECTION III	INTERFACE	-296-
SECTION IV	ALIGNMENT/MAINTENANCE	-302-
CHAPTER 11	SCANNER, MECHANICAL, INFRARED	-306-
SECTION I	GENERAL DESCRIPTION	-307-
SECTION II	FUNCTIONAL DESCRIPTION	-309-
SECTION III	INTERFACE	-318-
SECTION IV	ALIGNMENT/MAINTENANCE	-326-
CHAPTER 12	DETECTOR/DEWAR INFRARED	-328-
SECTION I	GENERAL DESCRIPTION	-329-
SECTION II	FUNCTIONAL DESCRIPTION	-331-
SECTION III	INTERFACE	-340-
SECTION IV	ALIGNMENT/MAINTEANCE	-353-
CHAPTER 13	LIGHT EMITTING DIODE ARRAY, IR	-362 -
SECTION I	GENERAL DESCTIPTION	-363-
SECTION II	FUNCTIONAL DESCRIPTION	-364-
SECTION III	INTERFACE	-365-
SECTION IV	ALIGNMENT/MAINTENANCE	-372-
APPENDIX I	THE EFFECT OF ATMOSPHERE ON ENERGY TRANSMISSION	-I-1-
APPENDIX II	ULTIMATE PERFORMANCE OF AN ELEMENTAL DETECTOR VIEWING A BAR PATTERN	-II-1-

CHAPTER 1

TYPICAL COMMON MODULE SYSTEM

SECTION I

INTRODUCTION

1.1 GENERAL

This designers handbook was prepared under Contract No. DAAG53-75-C-0178 by Philips Audio Video System Corp., Government Systems Division, Mahwah, New Jersey for the Night Vision Laboratory, Fort Belvoir, Virginia.

1.2 PURPOSE AND SCOPE

The purpose of this manual is to provide information that will aid the system designer in designing a Forward Looking Infrared (FLIR) or Thermal Imaging System using the common modules.

Chapter 1 provides design information on a "typical" system based on the use of common modules. This includes a functional description of a typical common module system and a system thermal discussion.

Chapters 2 through 13 provide detailed design information on each of the common modules. Items discussed include; general description, technical specifications, theory of operation, electrical and mechanical interface information, design limitations, and alignment/maintenance information. Schematic diagrams, block diagrams, outline drawings and photographs of the modules are included.

The common modules included in this manual are as follows:

Chapter	Module	USAECOM P/N
2	Preamplifier, Video, Infrared	SM-D-773663
3	Postamplifier/Control Driver, Video, Infrared	SM-D-773900
4	Auxiliary Control, Video, Infrared	SM-D-773896
5	Regulator, Bias, Infrared	SM-D-773914
6	DC/AC Inverter Assembly (P/O Cooler/Inverter, Infrared)	SM-D-773433
7	Modular Cooler Assembly (P/O Cooler/Inverter, Infrared)	SM-D-773683

Chapter	Module	USAECOM P/N
8	Scan and Interlace, Infrared (60Hz)	SM-D-773894
9	Collimator, Visual, Infrared	SM-D-773397
10	Imager, Optical, Infrared	SM-D-773419
11	Scanner, Mechanical, Infrared	SM-D-773885
12	Detector/Dewar, Infrared	SM-D-773781
13	Light Emitting Diode Array, Infrared	SM-D-773638

The following is a list of the modules and applicable specification:

Module	Specification
Scanner, Mechanical IR	B2-28A050107
Scan & Interlace IR	B2-28A050120
Collimator, Visual IR	B2-28A050105
Preamplifier, Video IR	B2-28A050106
Post Amplifier, Video IR	B2-28A050116
Auxiliary Control, Video IR	B2-28A050117
Bias Regulator, IR	B2-28A050118
Imager, Optical IR	B2-28A050104
Modular Cooler	B2-28A050108
Detector/Dewar IR	B2-28A050102
Light Emitting Diode	B2-28A050103

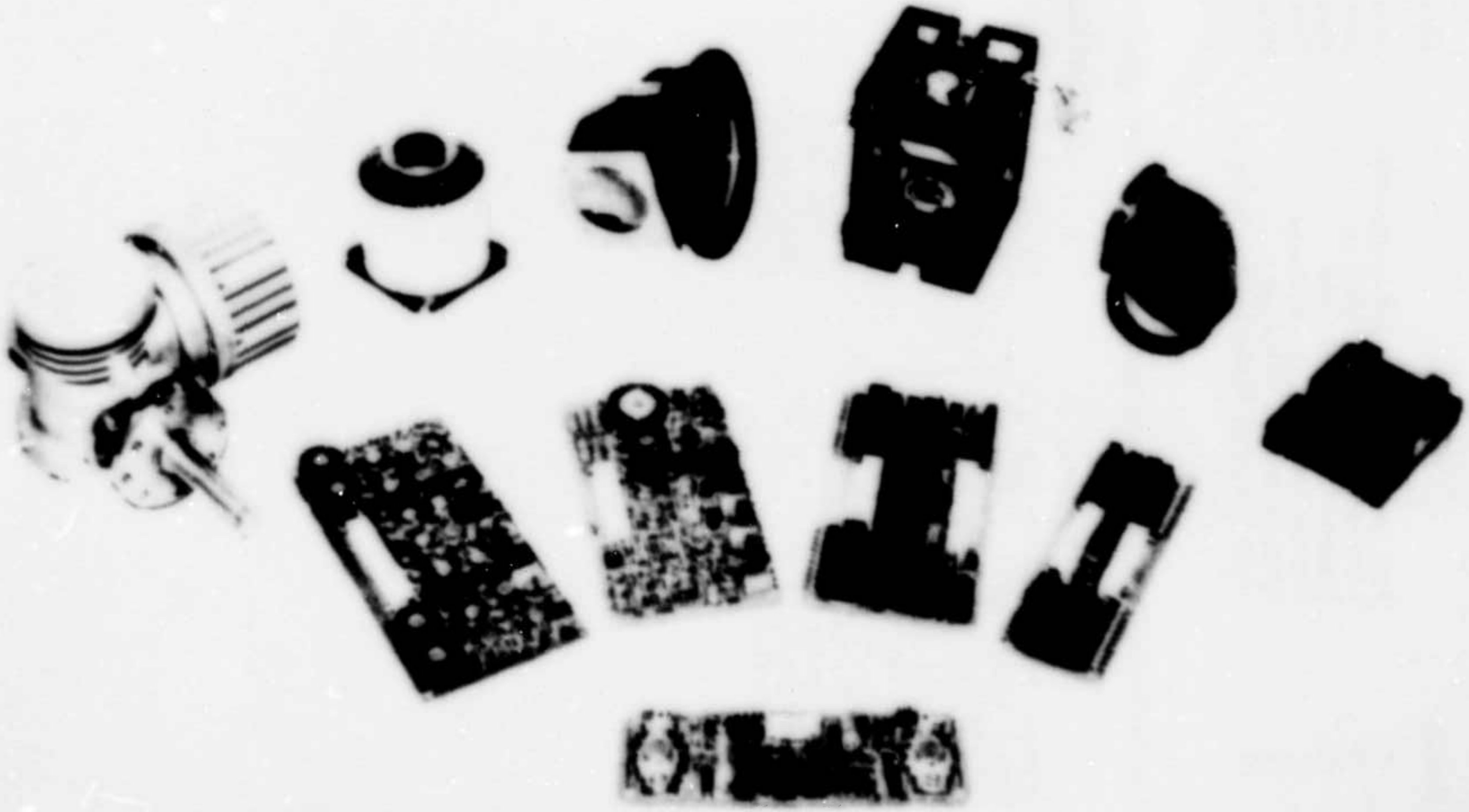


Figure 1-1. Common Modules

SECTION II

FUNCTIONAL DESCRIPTION

2.1 TYPICAL COMMON MODULE SYSTEM

A functional description of a typical common module system as shown in the block diagram of Figure 2-1 follows. Infrared energy from the viewed scene is recieved by an afocal, magnifying, infrared lens having 3:1 step zoom capability. A recollimated beam from the afocal lens impinges on the front-surfaced glass mirror of the scanner module. The energy is reflected to the IR imaging module which focusses it on the detector array. The common module elements, starting from the output of the afocal lens form a fixed electro-optical system since the physical dimensions of the common module elements are themselves fixed. Summarizing briefly; the elements are as follows:

(1) Detector: Array of 180 vertically oriented elements of Mercury Cadmium Telluride (HgCdTe). The array is formatted for a 2:1 interlace. The spectral band is 7.5 to 12.0 micron.

(2) IR Imager:

- Effective focal length - 2.669 in.
- F/Number - with no external stop the f/number is f/1.6, set by the aperture of the first lens element
- Field of View - sufficient to fill a field of view of 6.89° (corresponding to 80 detector elements or 160 resolution elements taking the 2 to/1 interlace into account).

(3) Scanner: The mechanical oscillation of the mirror can be adjusted to give an active scan angle up to 10° (5° to each side of center), with a scan efficiency of at least 70% as described in the B2 specification.

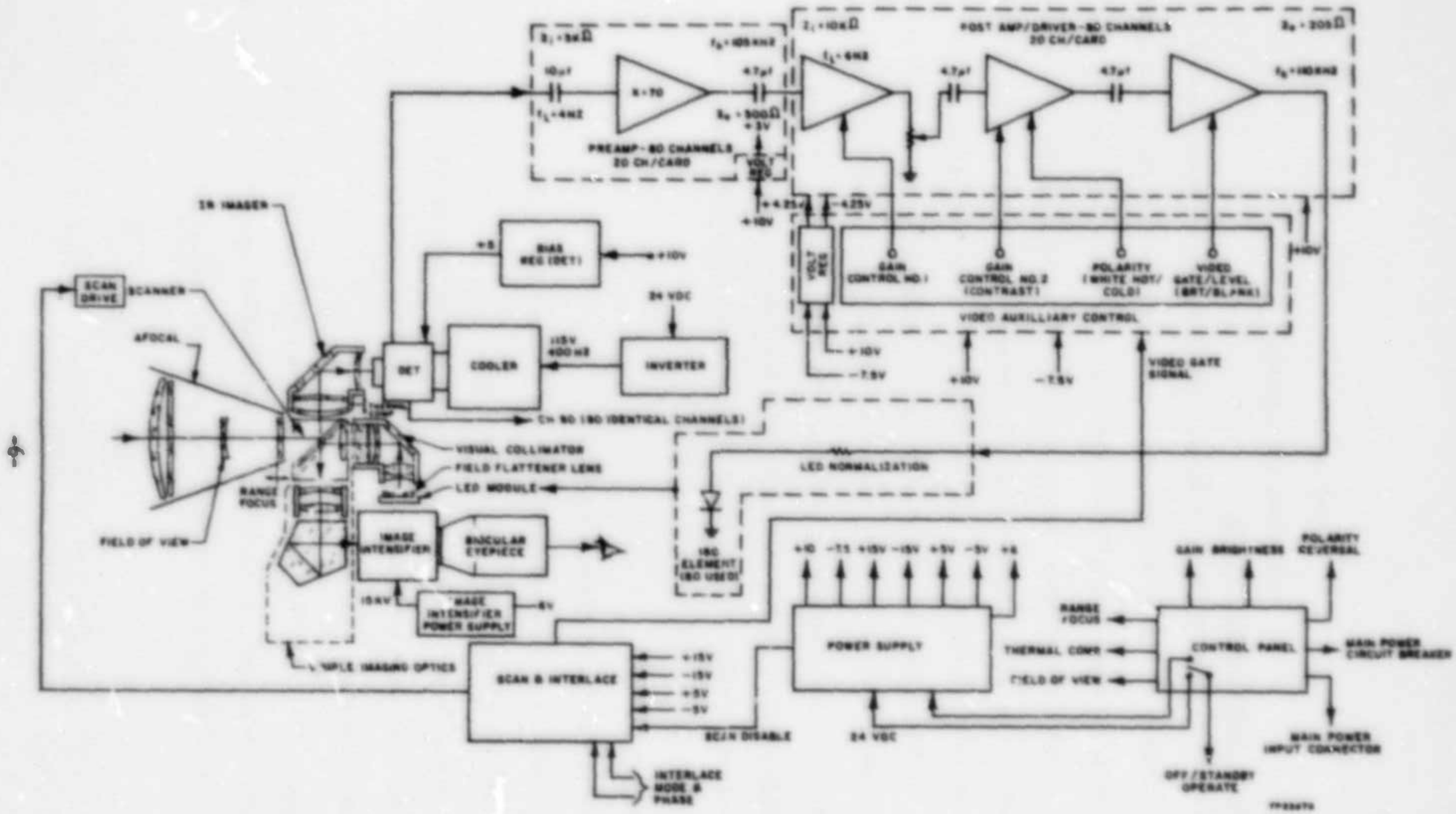


Figure 2-1 Typical Common Module System Functional Block Diagram

(4) Scan and Interlace Electronics:

Provides mirror motion drive. At the end of each scan the scan mirror nods about an axis which is 30° off the vertical. This motion provides the required interlace through a vertical tilt. A horizontal component derived from the nodding motion provides horizontal translation of the phase lens to correct for electronic phase shifts in the detector signal channels.

(5) Cooler: The detectors are cooled to approximately 77°K by a Stirling cycle cooler operating from 115 volts, 400 Hz.

(6) Preamplifier: The preamplifier modules provide a gain of 70 volts/volt. The electrical signal from each detector is AC coupled to a low noise preamplifier. There are 20 preamplifier channels per card.

(7) Post amplifiers: The post ampiifiers consist of 3 capacitively coupled stages. The first two stages have electronically controlled gain and polarity. A potentiometer between the electrically identical first and second stages is adjusted to normalize detector responsivity variations. Gain control and polarity reversal commands are provided to them for all channels in parallel by means of the auxiliary control module. In combination, gain control commands 1 and 2 provide a gain (contrast) variation of 30 dB. The gain command 1 circuitry also provide temperature compensation to assure gain stability over varying temperature conditions. The third stage of each circuit is the LED driver. The DC level of the output of this stage is electrically controlled to provide display brightness control and end-of-scan blanking.

(8) LED Display: Outputs from the Post Amplifier boards are fed to the LED module. Resistors are contained within the LED module in series

with each LED to normalize the brightness of each element, assuring display uniformity. Visible light from the LED module is collimated by the Visual Collimator module. The collimated beam is passed through a phase lens to the back of the scan mirror.

(9) Image Intensifier: Since there is a one-to-one correspondence between the detector elements and the LED display elements, and since both the scene and the display are scanned by the same mirror, a visual representation of the infrared scene is imaged on the face of the image intensifier tube. After intensification the image is viewed through a biocular eyepiece. The purpose of the phase lens, which moves with the outer (interlace) gimbal of the scanner, is to optically correct for phase jitter of the image which occurs due to the back and forth scan and finite electronic bandwidth.

It should be noted that the Image Intensifier shown in this typical system is not needed in all systems. The visual image may be focused on the target of a TV camera tube for use with a TV display system. If direct viewing is desired and the image is bright enough to meet the particular system requirement without intensification, an eyepieve and visible imaging optics can be designed for use without an intensifier.

2.2 OPTICAL SYSTEM

The optical system is designed to provide a two dimensional infrared scan in the 7.5 to 12 micron region and to present a converted visual image of the infrared scene to an observer. Figure 2-2 is an isometric illustration of a thermal viewer utilizing all the optical elements of the common module. The first element in the system is a collector lens which will define the effective f/number of the infrared optical subsystem. In many applications a change of magnification is required, for wide field and narrow field viewing applications. Since the scan mirror requires a parallel bundle of rays, the front end elements must be an afocal design. A simple two step zoom lens can be accomplished by moving one of the lens elements comprising the afocal subsystem.

The scan mirror is a two sided mirror which oscillates in the azimuthal direction. The infrared imager collects the collimated scanned bundle and focusses the IR energy on the 180 element linear detector array. The detector is fabricated from elements of HgCdTe. Each vertical element is followed by a blank space for interlacing purposes. Interlacing is accomplished by a vertical displacement of the mirror. The displacement magnitude corresponds to a single detector element. A bidirectional scanning action is obtained by observing the IR scan on the forward and return cycles of the mirror. During the return cycle the mirror is deflected in elevation to effect the interlace scan. Several possible scan motions are shown in Figure 2-3. Figure 2-3a is a 2 to 1 forward interlace. Figure 2-3b is a 2 to 1 reverse interlace and Figure 2-3c is a 1 to 1 interlace. The 1 to 1 interlace differs from the 2 to 1 interlace in that the mirror is displaced in the elevation direction after a complete mirror oscillation cycle.

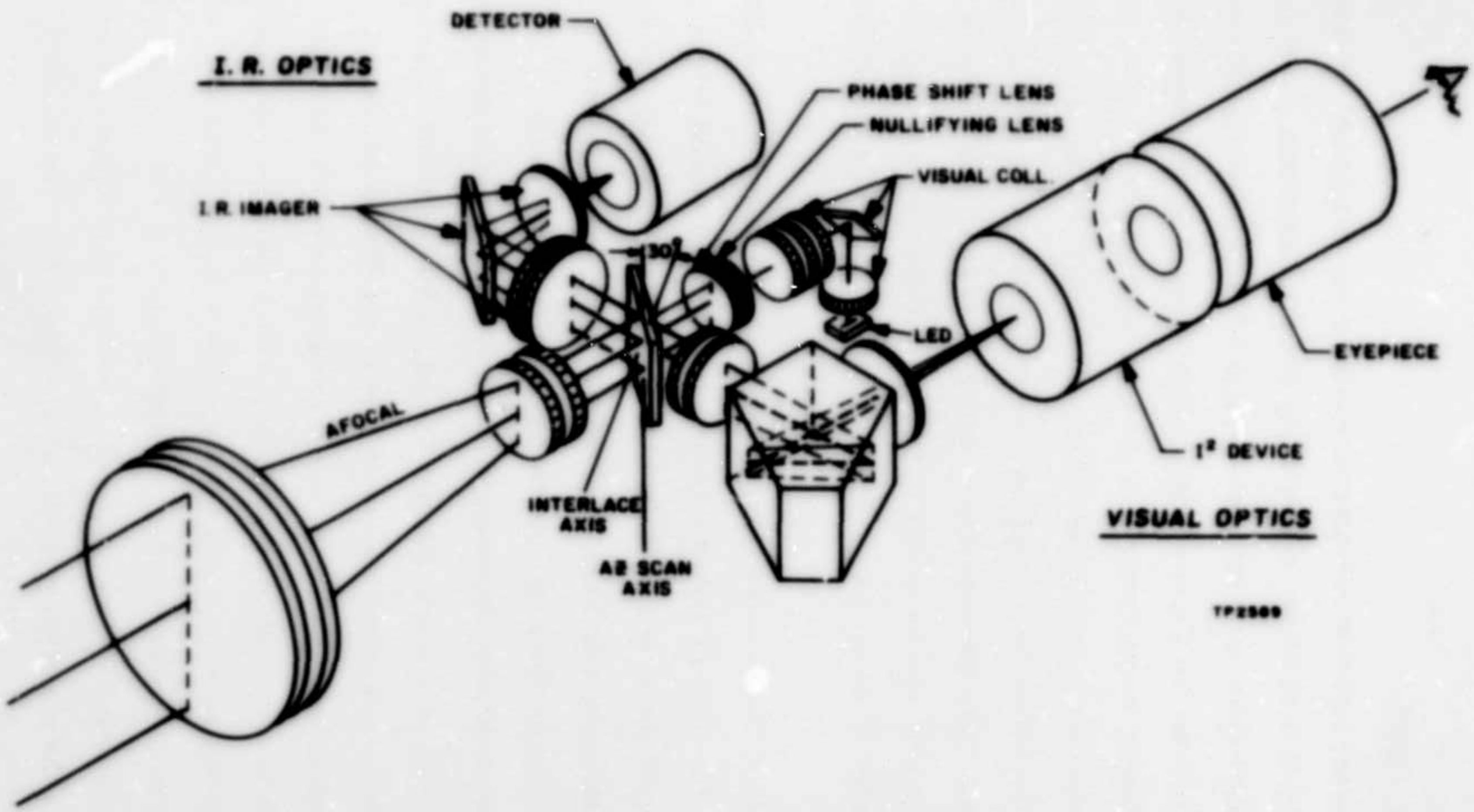


Figure 2-2 Visual Optics Physical Configuration, Typical Common Module Imaging System

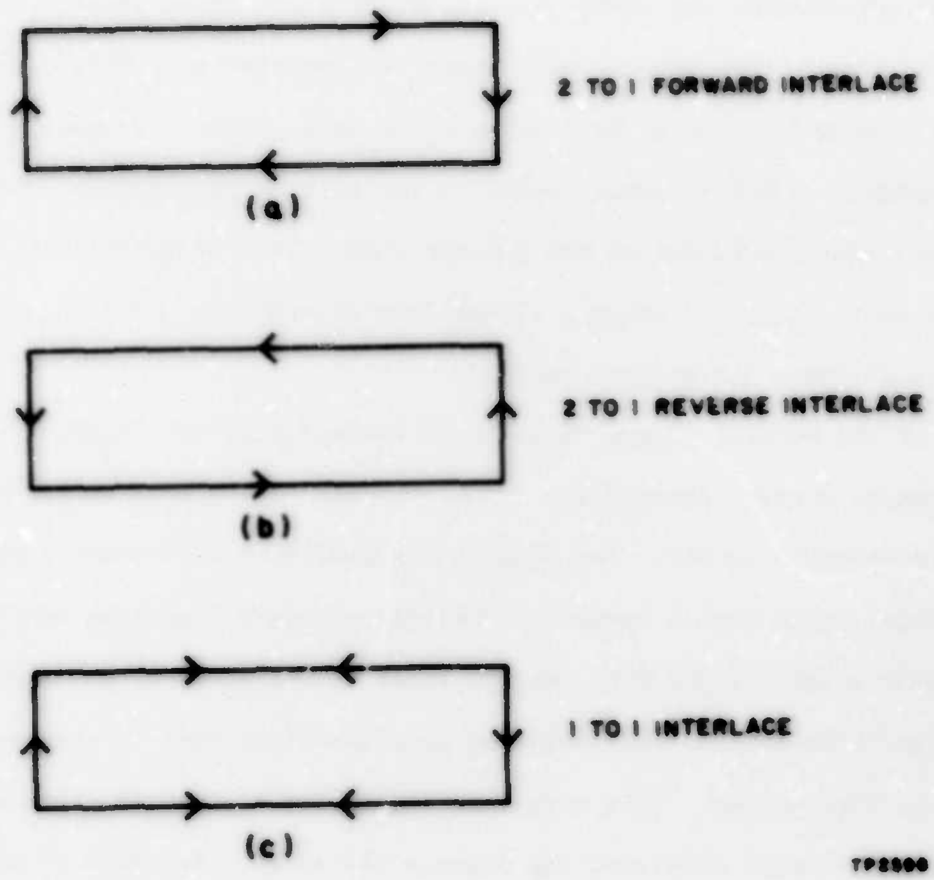


Figure 2-3 Scan Interlace Configurations

The bidirectional scan mirror is an excellent way to optimize scan efficiency but it is not without its attendant problems. Electronic phase shift in the amplifier chain is proportional to frequency, and will result in an information delay at the output. The phase delay provided by scanning a single point source in a single scan line is shown in Figure 2-4. The reverse scan accentuates the delay by a factor of 2 and would cause considerable blurring of the picture without some means of compensation. Phase shift compensation is provided optically by a phase shift lens which is a weak lens mechanically oscillated in a small lateral shift in the azimuth direction by means of a mechanical linkage actuated at the two end scan points of the mirror. Since the phase shift lens will cause a slight beam divergence, a nullifier lens is used to recollimate the optical bundle.

Each of the detector elements as it is scanned over the field of view by the scanner mirror, generates a signal representative of a single scan line in the picture raster. The signals are amplified sufficiently to drive an LED linear array with a number of vertical elements identical to that of the detector array. Light from the LED array is collected by a visual collimating lens which directs the resulting parallel light rays to the reverse side of the scan mirror. This visual analog of the scanned IR scene will be presented to a viewer observing the scanned LED array. In order to obtain an erect image with proper left to right orientation, for the final output viewing, the entire optical train in both the infrared and visual portions must be examined from the stand point of image inversions, and reversions due to lenses and mirrors. It should be borne in mind in designing any system that a relay or reimaging lens results in inverting, and reverting the image. A single 90° mirror fold changes left/right into up/down, and a periscope action or two successive 90° folds, results in the proper up/down and left/

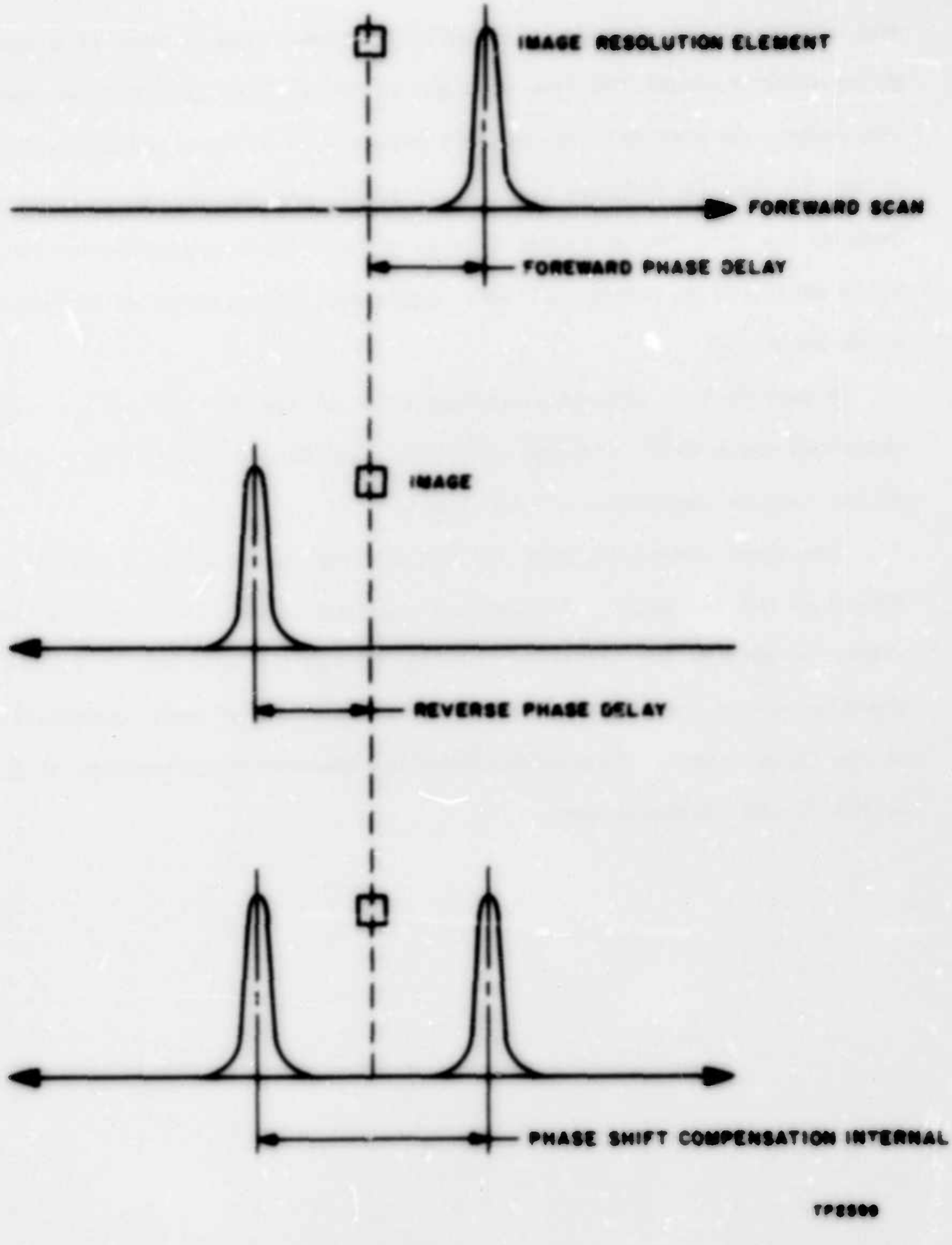


Figure 2-4 Phase Shift Resulting from Forward and Reverse Scan

and left/right orientation. In the system shown, use is made of a penta-prism which deviates the line of sight by 90° without inverting or reversing the image. It also has the valuable property of being a constant deviation prism, in that it deviates the line of sight through the source angle regardless of its orientation to the line of sight. The penta-prism is used where it is desirable to produce a 90° deviation, without having to orient the prism precisely.

Figure 2-5 is a schematic configuration of the physical configuration described above which provides a valuable key toward understanding the action of the various components of the system.

The final viewing is done through an eyepiece mounted at the rear entrance of the IR imager. In most applications it will be important for the viewer to observe the target by looking through the eyepiece in a straight ahead manner so that the up/down and left/right are an exact correlation of the target scene. Figure 2-6 summarizes the optical principles as discussed in the foregoing test.

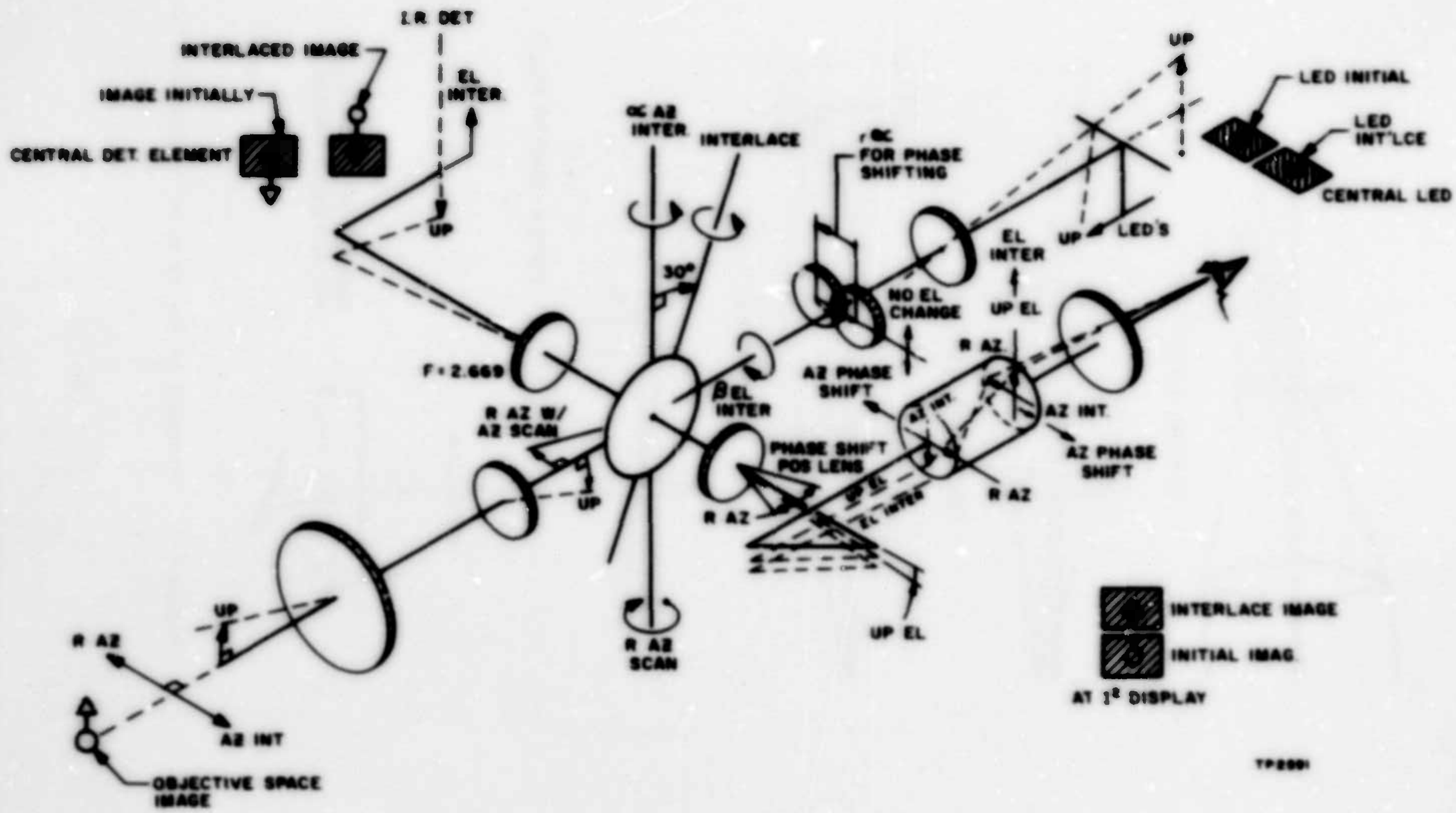


Figure 2-5 Schematic Configuration Typical Common Module Imaging System

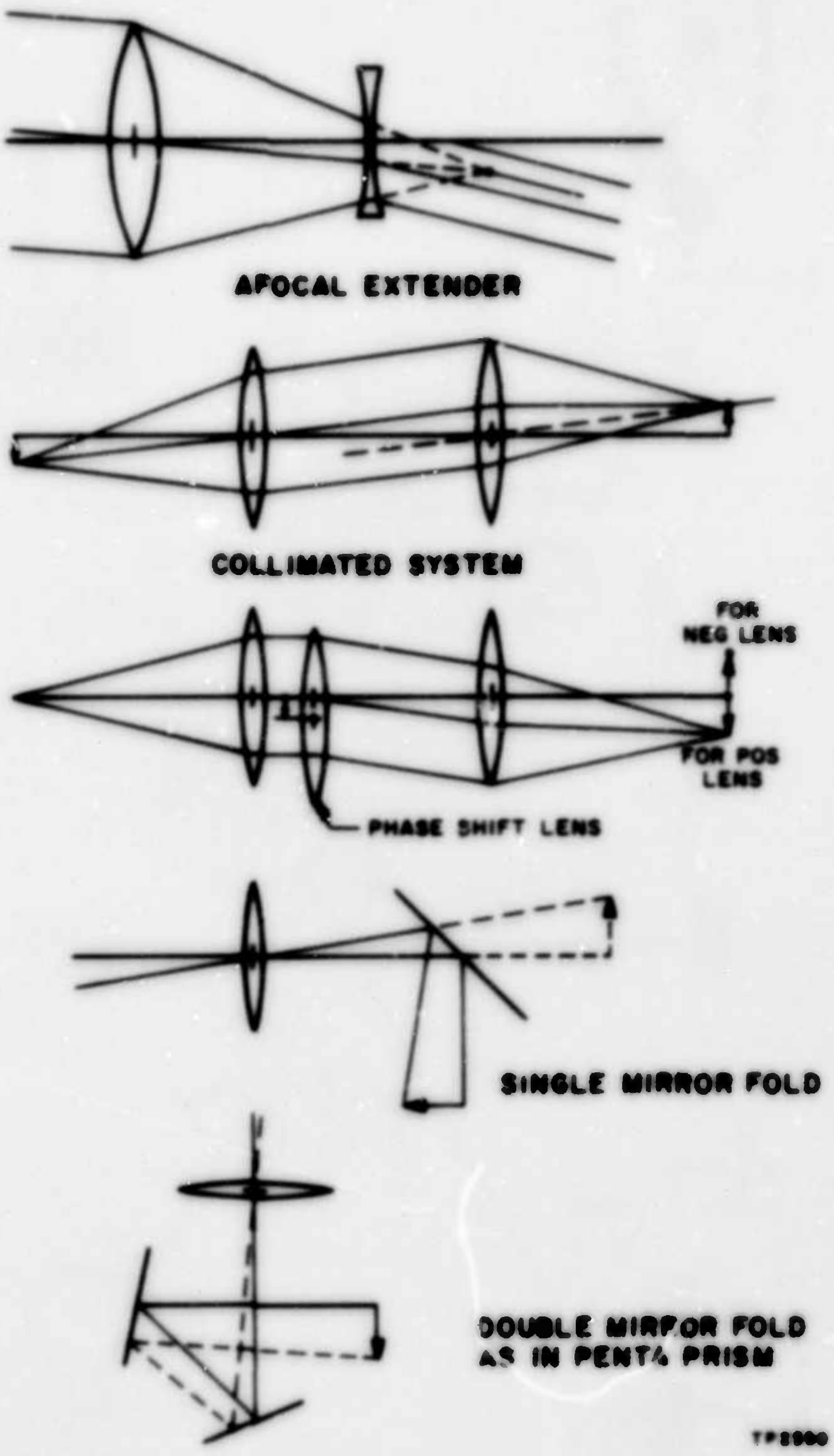


Figure 2-6 Principle of Operation of Typical Optical Elements

2.3 IMAGE PRESENTATION ANALYSIS

In a complex optical system consisting of a number of lens and mirror elements with several path deviations, an analysis of the image presentation at the output in terms of inversions, and reversions must be determined. Figure 2-7 shows the infrared portion of a typical infrared night sight which scans up through a periscope. The technique used for image presentation is to first layout a schematic showing the light path as diverted by the non-power surfaces such as a mirror or a prism. A left/right and up/down arrow diagram should be thus traced through the system. Next the lenses or mirrors which result in changing the beam divergence are inserted.

In the system shown in Figure 2-7 There is no image perturbation by the galilean afocal lens since its function is to produce a magnification of collimated space for the scanner proportional to the afocal reduction. However the imaging lens produces a single inversion and reversion of the image.

The effect of the visual optical system of Figure 2-8 will now be analyzed. We start by fixing the azimuth and elevation directions in object space as shown by the arrows. Again we determine the effect of the non-power path diverting devices without the lenses in place. The collimating and imaging lens act as a single relay lens and produce both inversion and reversion of the image. Thus an erector lens is required for proper image presentation to a viewer observing through the eyepiece.

2.3.1 NUMERICAL EXAMPLE OF SYSTEM USING COMMON MODULES

An example of a typical system using the common modules is presented in order to determine some of the numerical optical relationships which must be taken into account. The viewer is to observe a scene which has a high and low magnification or narrow field and wide field of view. The high magnifi-

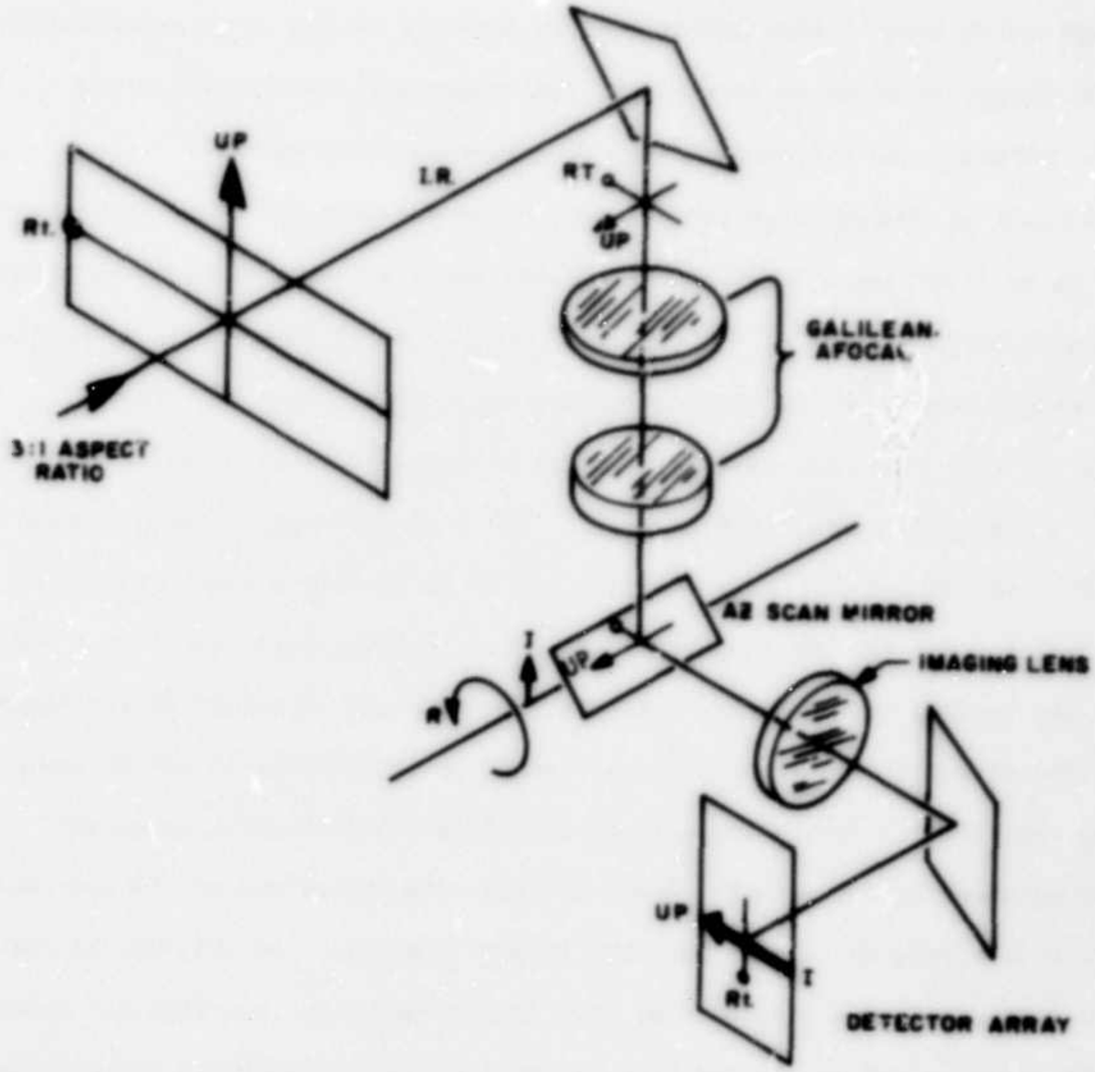


Figure 2-7 Infrared Optics Of Typical Night Sight

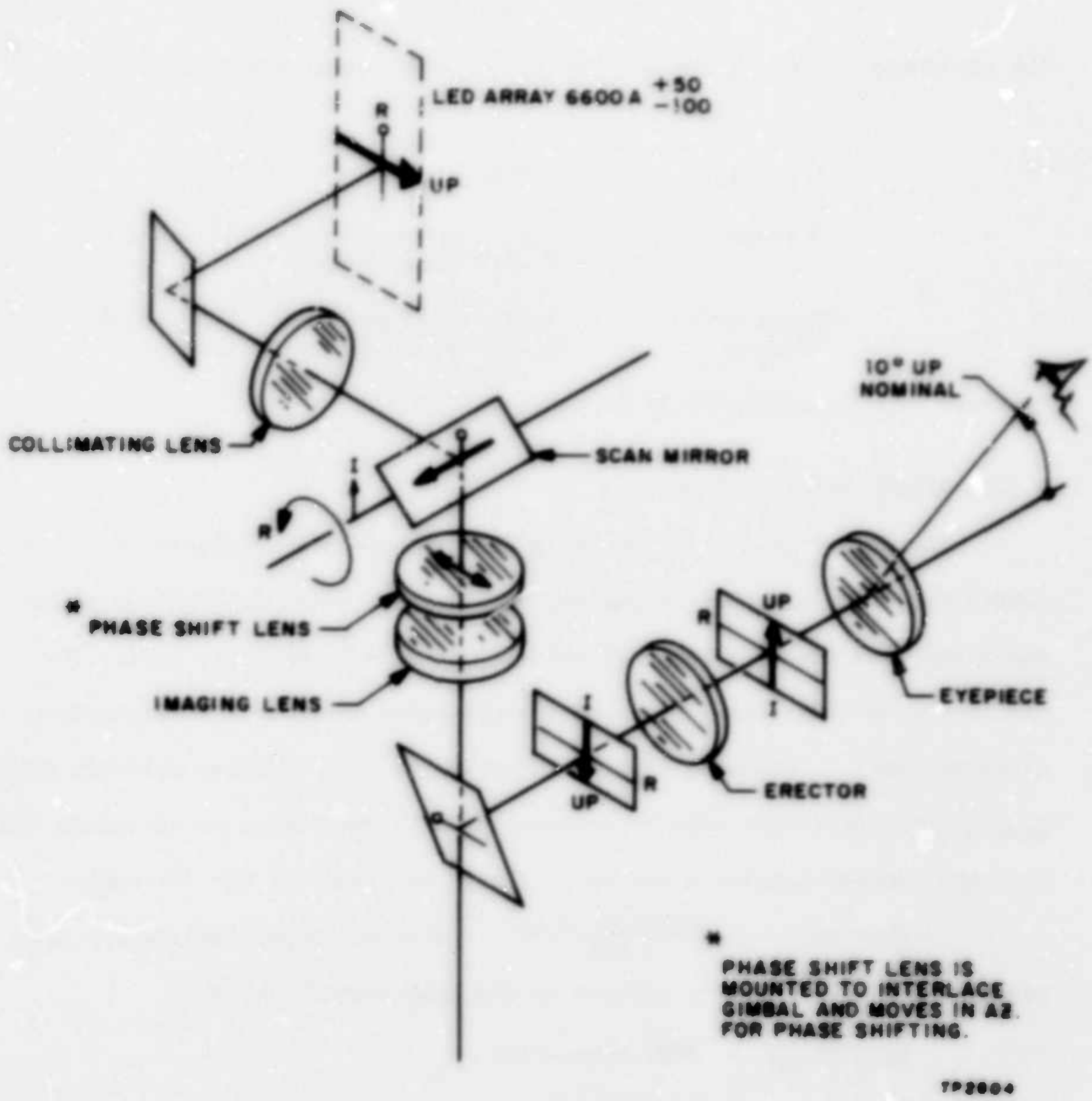


Figure 2-8. Visible Optics of Typical Night Sight

cation will be approximately 9.8X and the low manglfication 3.3X. The scanned fields of view in object space are:

Narrow field	-	1.5° elevation 3° azimuth
Wide field	-	4.5° elevation 9° azimuth

The constants in the system are defined by the common module elements:

LED array	-	.0375" x .00375
IR imager	-	2.5" clear aperture - 1st element 2.669" focal length
Visual collimator	-	1.58" clear aperture - 1st element 2.669" focal length

Physical angular excursion of mirror = 6.75°.

2.3.2 AFOCAL DESIGN PARAMETER

The design parameters of the afocal system will determine the focal length and clear aperture of the entrance pupil. A f/1.9 system as an example requires the exit pupil of the afocal to be 2.669/1.9 = 1.4". In the narrow FOV the afocal has 4.5X magnification given as 6.3" diameter entrance pupil. The wide FOV is 1.5X giving a 2.1" diameter entrance pupil.

Resolution - To obtain angular resolution in scanner space we calculate the detector element angular subtense in the focal length of the IR imager.

$$\text{Resolution} = \frac{\text{Detector size}}{2.669}$$

In object space the angular subtense of the resolution is divided by the zoom magnification or

$$\frac{\text{Resolution}}{4.5} = \text{NFOV resolution}$$

$$\frac{\text{Resolution}}{1.5} = \text{WFOV resolution.}$$

2.3.3 EYEPIECE ANGULAR SUBTENSE

The diagonal element in the scan field of 3° AZ x 1.5° EL is 3.35° in the narrow field. The eyepiece must be usable to an angle of $9.8 \times 3.35^{\circ} = 32.8^{\circ}$.

2.3.4 Figure 2-9 presents a typical optical system.

2.3.5 DIFFRACTION LIMIT

The diffraction limit defines the maximum resolution that can be obtained with an optical system. The best angular resolution that can be achieved is given by $\emptyset = \frac{2.44\lambda}{D}$ or in terms of the focal length and F/# $\emptyset = \frac{2.44\ f/\#}{x\ Fl}$. The F/# of the system is defined by the system optics. The F/# of the example system is F/1.9. The middle wavelength is 10 microns or 1×10^{-4} and the focal length is 6.78 cm. The diffraction limit is thus

$$\emptyset = \frac{2.44 \times 10^{-3} \times 1.9}{x\ 6.78} = .68 \times 10^{-3} \text{ rad.}$$

For the narrow field of view the afocal magnification is 4.5X and the diffraction limit is 0.15×10^{-3} rad. The WFOV has a magnfication of 1.5X giving a diffraction limit of 0.45×10^{-3} rad.

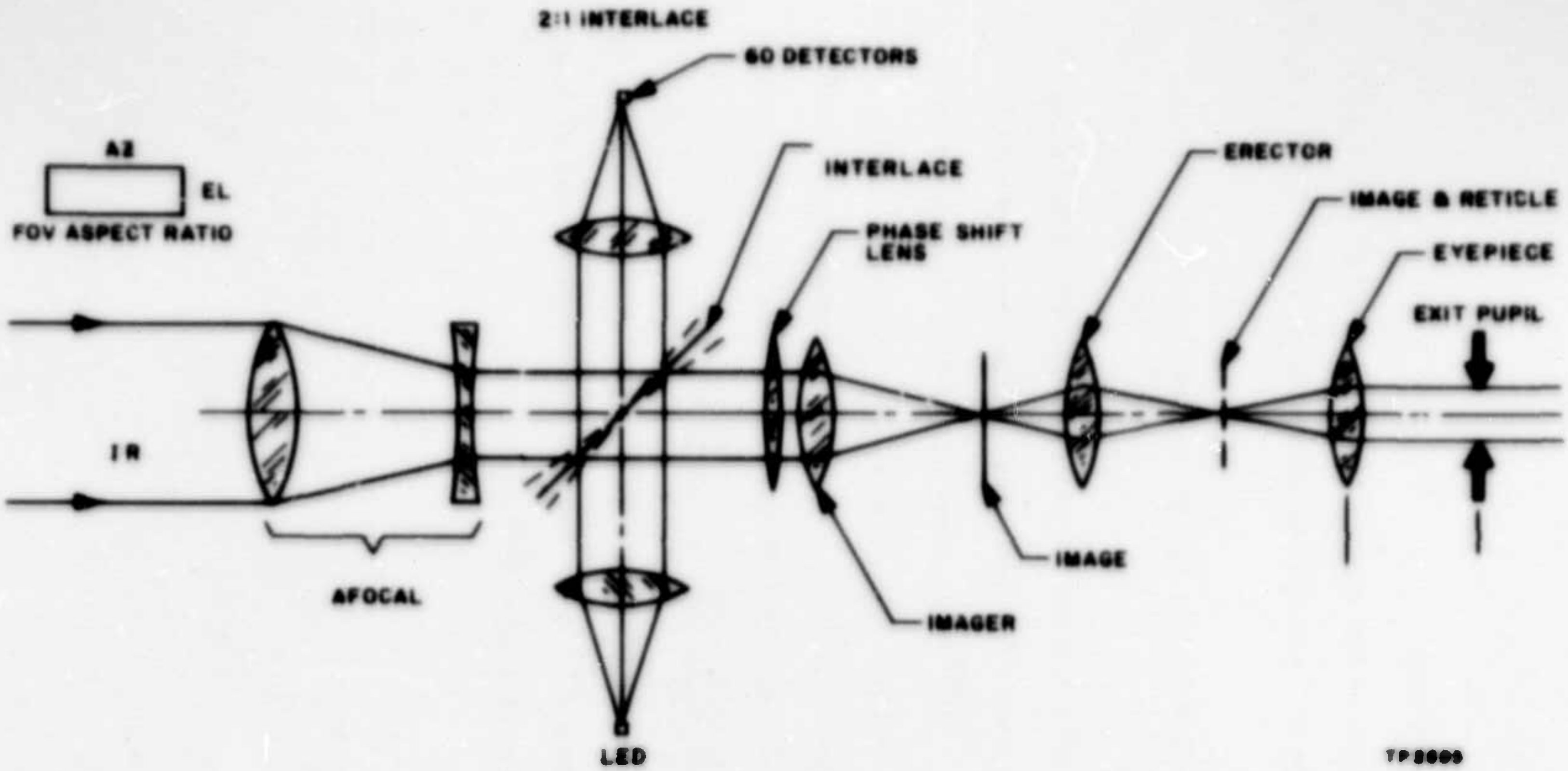


Figure 2-9 Typical Optical System

2.4 FLIR PERFORMANCE REQUIREMENTS

2.4.1 ESTABLISHMENT OF SCENARIOS

Thermal Imaging Systems or FLIR's are commonly used to detect, recognize and identify military threats under cover of darkness. For this handbook, we have considered likely targets to ranges of up to 9 kilometers.

Although there are many possible scenarios, there are always two critical parameters which impose certain requirements on the design of a FLIR: the characteristics of the target and of the intervening medium (atmosphere). In this section we discuss the manner in which these parameters affect the design of the sensor in terms of required resolution and sensitivity.

2.4.2 SCENE CONTRAST

Emissivity Differences

Table 2-1 shows the emissivity of common terrain features in the visible, airglow, near IR (3 - 5 microns), and far IR (8 - 14 microns). In general, objects become more emissive and hence less reflective as wavelength is increased.

It can be seen that emissivity values in the 3 - 5 micron region range from approximately 0.8 to 1 and in the 8 - 14 micron region, they range from 0.95 to 1. If an opaque target (transmissivity = 0) is at the same temperature as its background and the background has unit emissivity, the target will not be visible against the background, no matter what the target emissivity is. The emissive radiance of the target is decreased by decreasing the emissivity, and the radiance of the background reflected from the target will increase just enough to make the target as bright as the background, since the reflection coefficient = $1 - \epsilon$, where ϵ = emissivity.

TABLE 2-1. REFLECTANCE ρ AND EMISSIVITY ϵ OF COMMON TERRAIN FEATURES

	0.7-1.0 um	1.8-2.7 um	3-5 um	8-14 um
Green Mountain Laurel	ρ = 0.44	ϵ = 0.84	ϵ = 0.90	ϵ = 0.92
Young Willow Leaf (dry, top)	0.46	0.82	0.94	0.96
Holly Leaf (dry, top)	0.44	0.72	0.90	0.90
Holly Leaf (dry, bottom)	0.42	0.64	0.86	0.94
Pressed Dormant Maple Leaf (dry, top)	0.53	0.58	0.87	0.92
Green Leaf Winter Color--Oak Leaf (dry, top)	0.43	0.67	0.90	0.92
Green coniferous Twigs (Jack Pine)	0.30	0.86	0.96	0.97
Grass--Meadow Fescue (dry)	0.41	0.62	0.82	0.88
Sand--Hainamanu Silt Loam--Hawaii	0.15	0.82	0.84	0.94
Sand--Barnes Fine Silt Loam--So. Dakota	0.21	0.58	0.78	0.93
Sand--Gooah Fine Silt Loam--Oregon	0.39	0.54	0.80	0.98
Sand--Vereiniging-Africa	0.43	0.56	0.82	0.94
Sand--Maury Silt Loam--Tennessee	0.43	0.56	0.74	0.95
Sand--Dublin Clay Loam--California	0.42	0.54	0.88	0.97
Sand--Pullman Loam--New Mexico	0.37	0.62	0.78	0.93
Sand--Grady Silt Loam--Georgia	0.11	0.58	0.85	0.94
Sand--Colts Neck Loam--New Jersey	0.28	0.67	0.90	0.94
Sand--Mesita Negra--lower test site	0.38	0.70	0.75	0.92
Bark--Northern Red Oak	0.23	0.78	0.90	0.96
Bark--Northern American Jack Pine	0.18	0.69	0.88	0.97
Bark--Colorado Spruce	0.22	0.75	0.87	0.94

If the target is hotter than the background, the effective temperature difference, to a first approximation, will be the actual temperature difference decreased by the emissivity of the target.

It is assumed in these analyses that all emissivities equal 1.0. Therefore, the temperature differences used may be optimistic by about 20 percent in the 3 - 5 micron range, by 5 percent in the 8 - 12 micron range.

It should be noted that low emissivity materials such as polished metals may have emissivities as low as 10 - 15 percent. However, most objects encountered on the battlefield will be dirty, so that their emissivity will approach those given in Table 2-1.

Temperature Differences

Temperature differences in the infrared may vary from 0°K to tens of degrees depending on conditions. For example, if a tank is exposed to the elements, not operating, and out of the sun for several hours, there is essentially no temperature difference between the tank and its background. However, if the tank has been operating, the tread and engine compartments may heat up to 10 - 20° above ambient, while the exhaust pipe may be 100° above ambient and the turret still at ambient. If the cannon has been fired, it too may be 100° above ambient. Therefore, the target signature, or the target scene temperature difference, must be treated as a variable.

Scene Energy Content

Figure 2-10 shows natural illumination levels and the radiance of a 300° blackbody. It can be seen that the number of photons available for imaging in the infrared (3-5 μm or 8-14) far exceeds that available for the visible even in full moonlight. However, it is not so much the magnitude of the photon flux which concerns us, but rather the difference between the amount coming

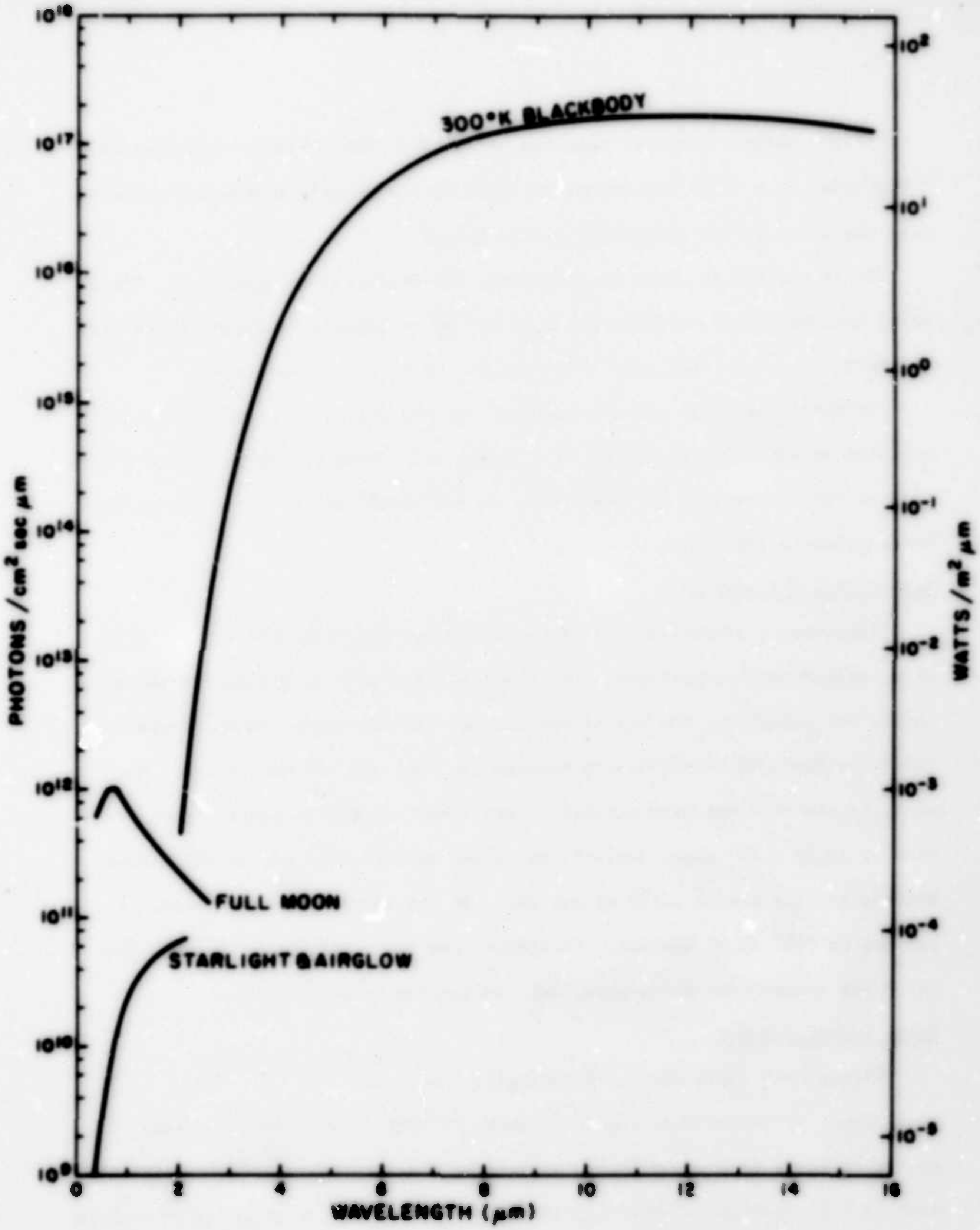


Figure 2-10. Bottom: Spectral Irradiance of a Night Scene Illuminated by Starlight and Airglow; Center: Spectral Irradiance of a Night Scene Illuminated by a full moon; top: Spectral Radiant Emittance of a 300°K Blackbody

from the target and the amount from the background which will determine how clearly the target will be perceived.

As mentioned earlier, this difference is determined primarily by the difference in reflection coefficients in the visible, and by temperature difference in the IR.

Figure 2-11 shows the differential spectral radiance for a one degree temperature difference. Differential spectral radiance in the 8 - 14 μm band is an order of magnitude higher than in the 3 - 5 μm band. This does not mean that operation in the 8 - 14 μm region is an order of magnitude better than in the 3 - 5 μm region.

So far, we have considered only signal and not noise. The magnitude of the radiance levels are so large that statistical fluctuations become comparable to the differential radiance providing signal. Figure 2-12 shows S/N as a function of wavelength with the statistical fluctuation of the signal as the sole noise source.

It can now be seen that the background S/N reaches a maximum at 8 μm and that the S/N in the 8 - 14 μm region is larger than in the 3 - 5 μm region for targets at approximately 300°K. However, as shown in the next section that weather effects are less severe in the 8 - 14 μm region than in the 3 - 5 μm region.

In general, at long ranges or in foul weather, when weather substantially degrades signal, the 8 - 14 μm region will perform much better than the 3 - 5 μm region. At close ranges or in clear weather operation at 8 to 14 μm is only slightly better.

2.4.3 ATMOSPHERIC TRANSMISSION

Loss of energy and contrast caused by the atmosphere stems from two mechanisms, absorption and scattering.

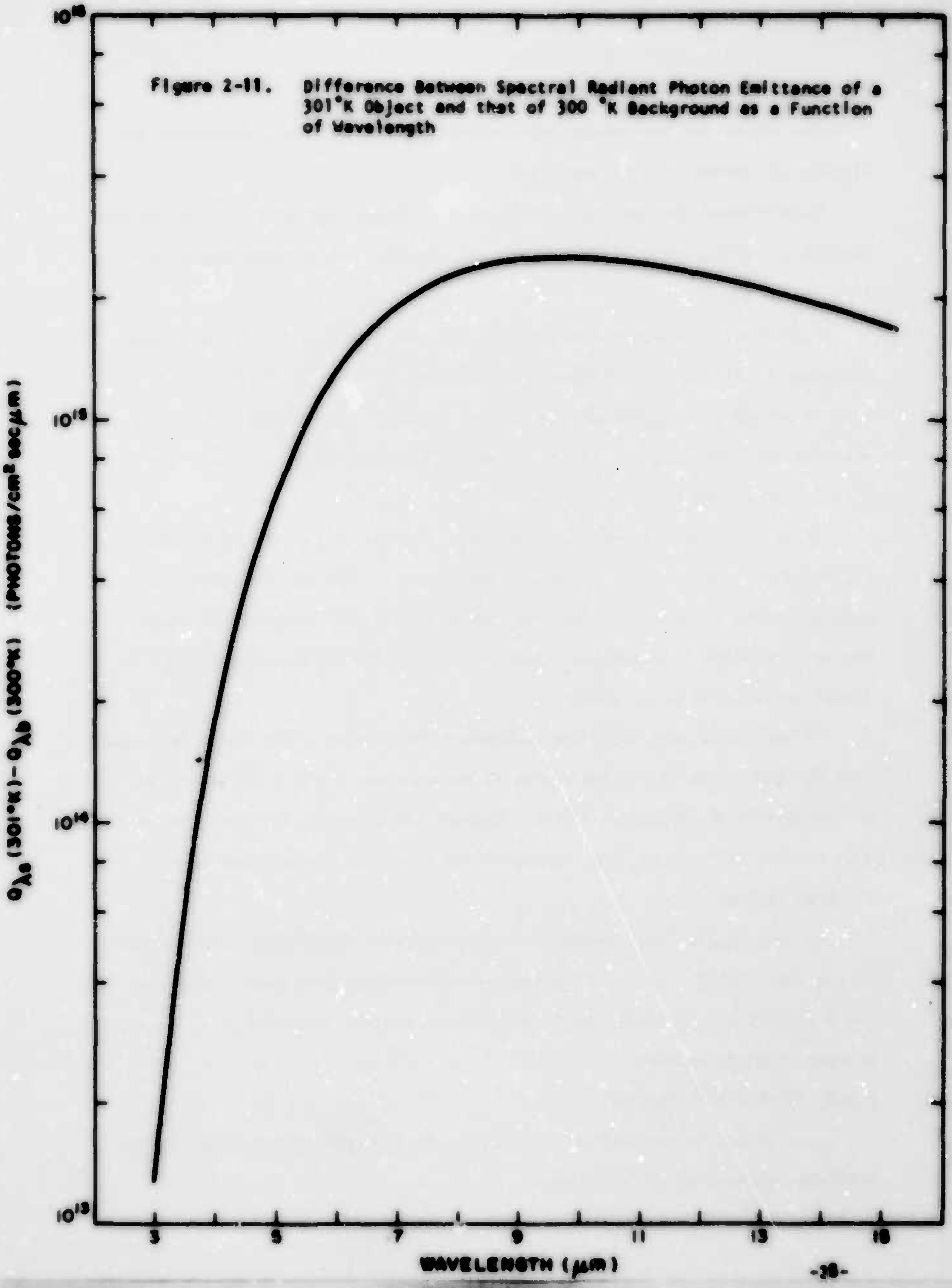


Figure 2-11. Difference Between Spectral Radiant Photon Emittance of a 301°K Object and that of 300 °K Background as a Function of Wavelength

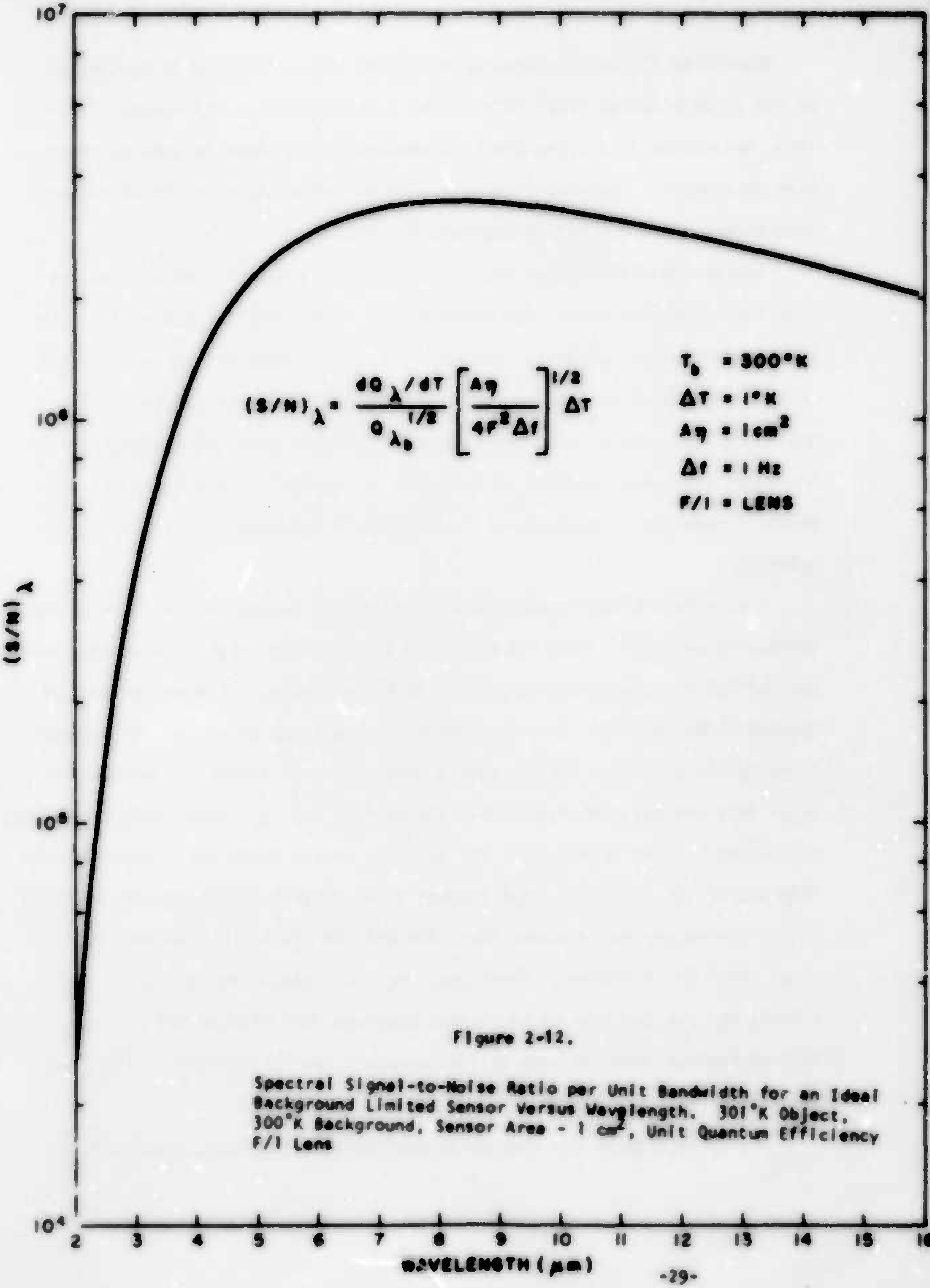


Figure 2-12.

Spectral Signal-to-Noise Ratio per Unit Bandwidth for an Ideal Background Limited Sensor Versus Wavelength. 301°K Object, 300°K Background, Sensor Area - 1 cm^2, Unit Quantum Efficiency F/1 Lens

Absorption is due to resonance of photon energy (related to wavelength by hc/λ) with energy level differences in atmospheric constituents. Therefore, absorption is discontinuous in wavelength and shows no general trend with wavelength. There are, however, regions where there is little resonant absorption; these are called atmospheric windows.

Scattering differs from absorption in that it does not extract energy from the signal but merely redistributes it. The effect is essentially the same as absorption, since the energy which is scattered out of the field of view of the sensor is lost to it. Multiple scattering will cause a point source to look like a disc, hence decreasing resolution. This effect of multiple scattering, because it is small, is ignored in this analysis. Appendix I contains an analysis of the effects of atmosphere on energy transmission.

Scattering is continuous with wavelength and depends on the size of the scattering particle. When the particle is much larger than a wavelength (Mie scattering) the scattering is uniform with wavelength. This is the case of visible light scattered by a fog; the scattered light is white. As the scattering particle becomes smaller than a wavelength the scattering coefficient drops very rapidly with wavelength, approaching a $1/\lambda^4$ relationship (Rayleigh scattering.) This is the case, for example, of air molecules scattering visible light; the scattered light appears blue. Figure 2-13 shows the particle size distribution for haze and fog. The peak for both distributions appears to be about 2 - 3 microns. Therefore, one would expect the scattering coefficient for fog and haze to be roughly constant (Mie scattering) for wavelengths shorter than the peak at 2 - 3 microns, and to fall off sharply for wavelengths beyond the peak.

Figure 2-14 shows the scattering coefficient of several types of fogs.

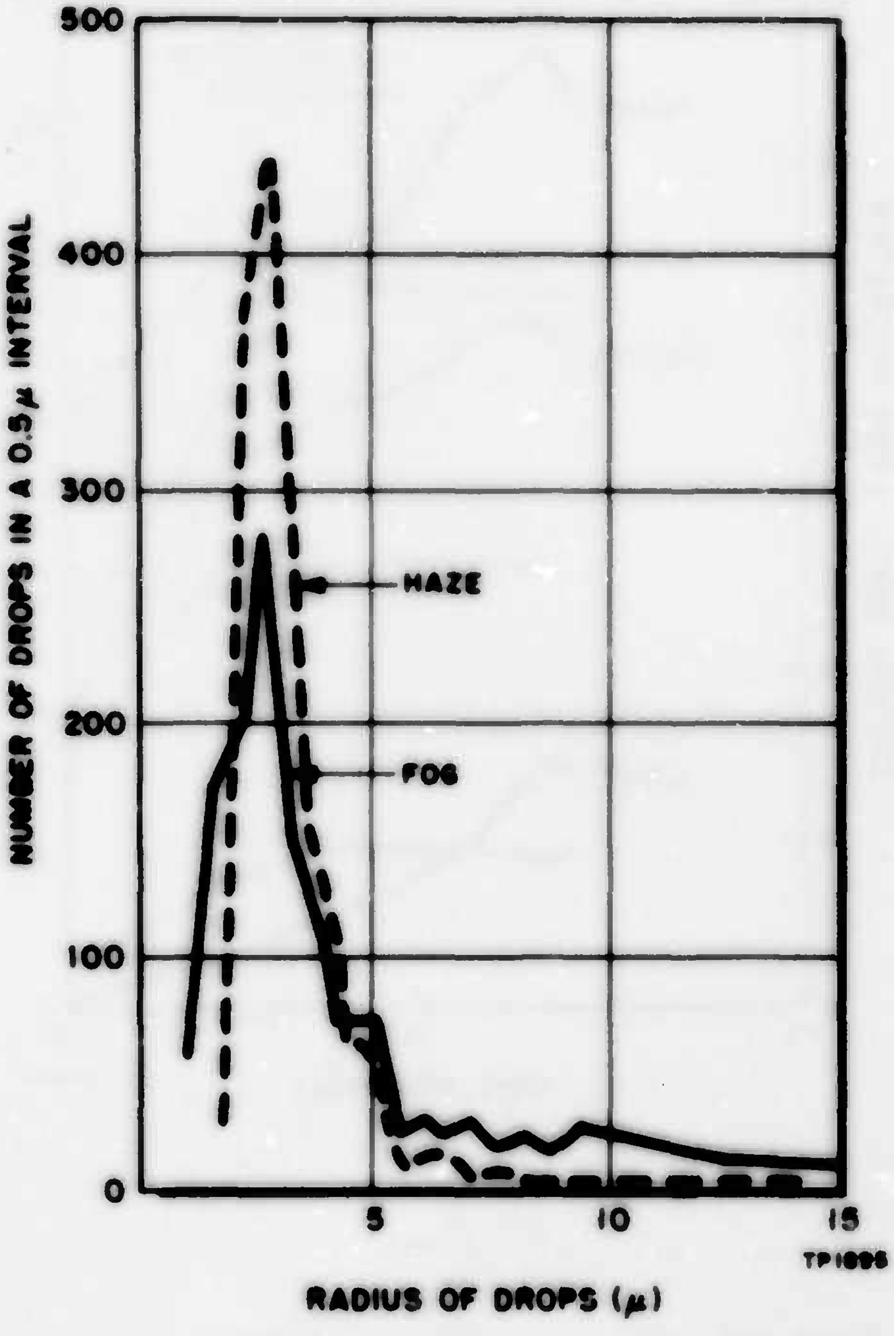


Figure 2-13. Particle Distribution for a Haze and a Fog

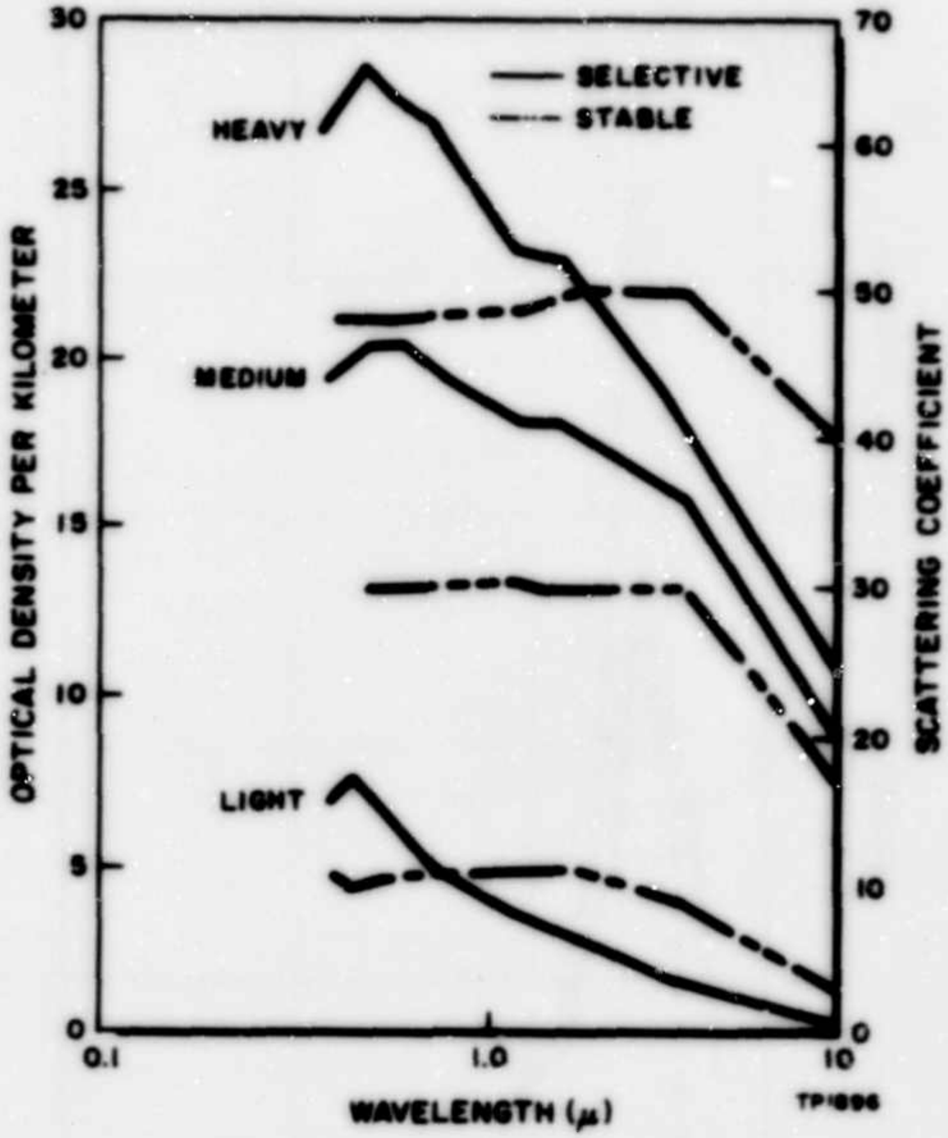


Figure 2-14. Scattering Coefficient of Several Types of Fog

Note that the behavior of stable fogs agree extremely well with that predicted above. The curves used to generate the data for this study are those labeled selective. These are characteristic of artificial smoke (e.g., battlefield smoke) as well as certain fogs. The three conditions are displayed as light, medium and heavy fog. Had the stable cases been used rather than the selective case the atmospheric attenuation would appear less severe for all wavelengths. However, the visible through 3 micron region would improve far more than the 10 micron region.

Figure 2-15 gives the scattering coefficient for the haze considered. Figure 2-16 through 2-20 show atmospheric transmission as a function of range and weather conditions. Note that in the infrared there are two regions of little atmospheric attentuation, 3 - 5 micron and 8 - 14 micron. Table 2-2 shows the relative frequency of occurrence of various night viewing conditions in the Eastern United States.

TABLE 2-2

Atmospheric Condition	Average Scattering .5 - 1.0 μ	Probability of Occurrence in Eastern U.S.*
Clear Air	3×10^{-5}/meter	.25
Haze (Light)	5×10^{-4}/meter	.40
Haze	2×10^{-3}/meter	.80
Light Fog	10^{-2}/meter	.90
Dense Fog	4×10^{-2}/meter	.98

*This probability is the percentage of night viewing time when the given, or better (i.e., lower), value of scattering coefficient can be obtained. Thus 80 percent of the time the scattering coefficient would be better than (less than) 2×10^{-3}/meter (haze).

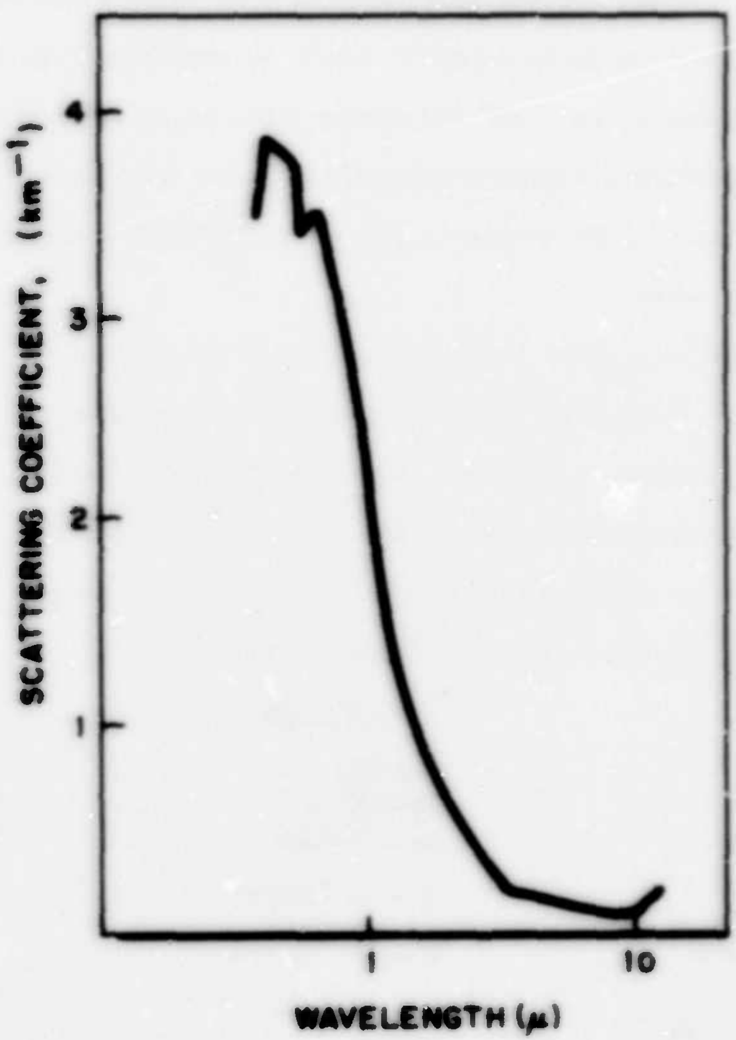


Figure 2-15. Scattering Coefficient of a Haze

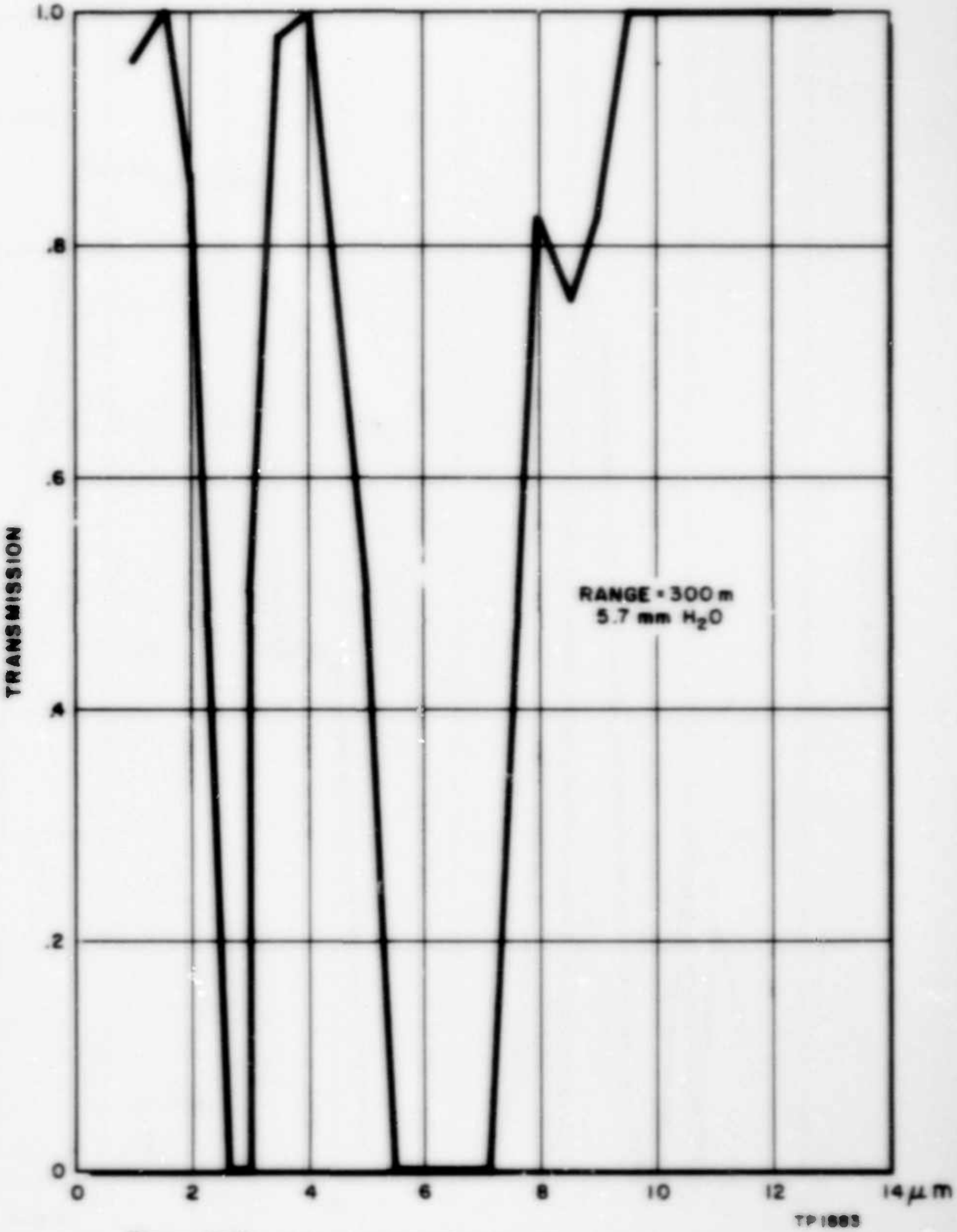


Figure 2-16. Spectral Transmission Through Clear Air

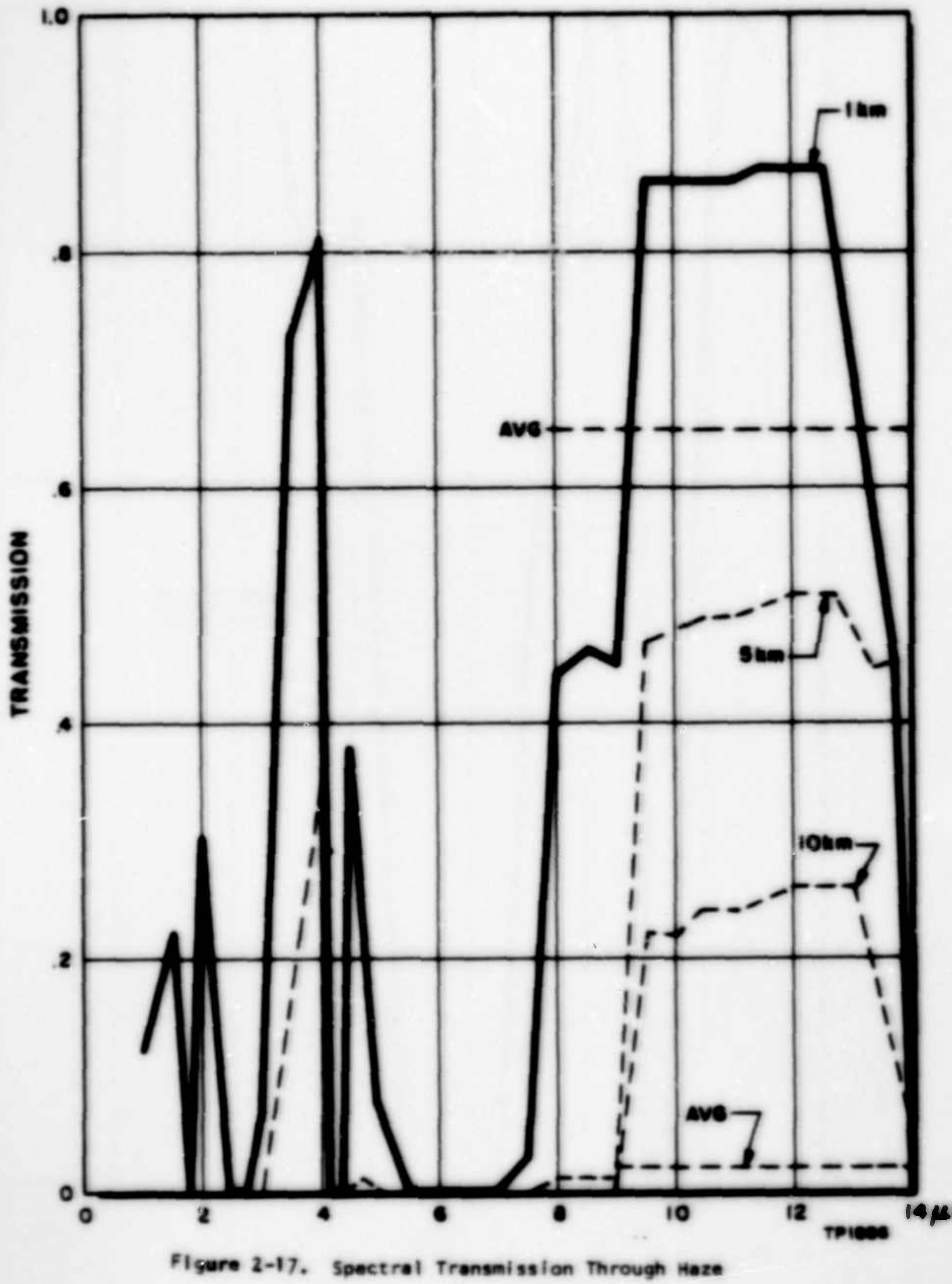


Figure 2-17. Spectral Transmission Through Haze

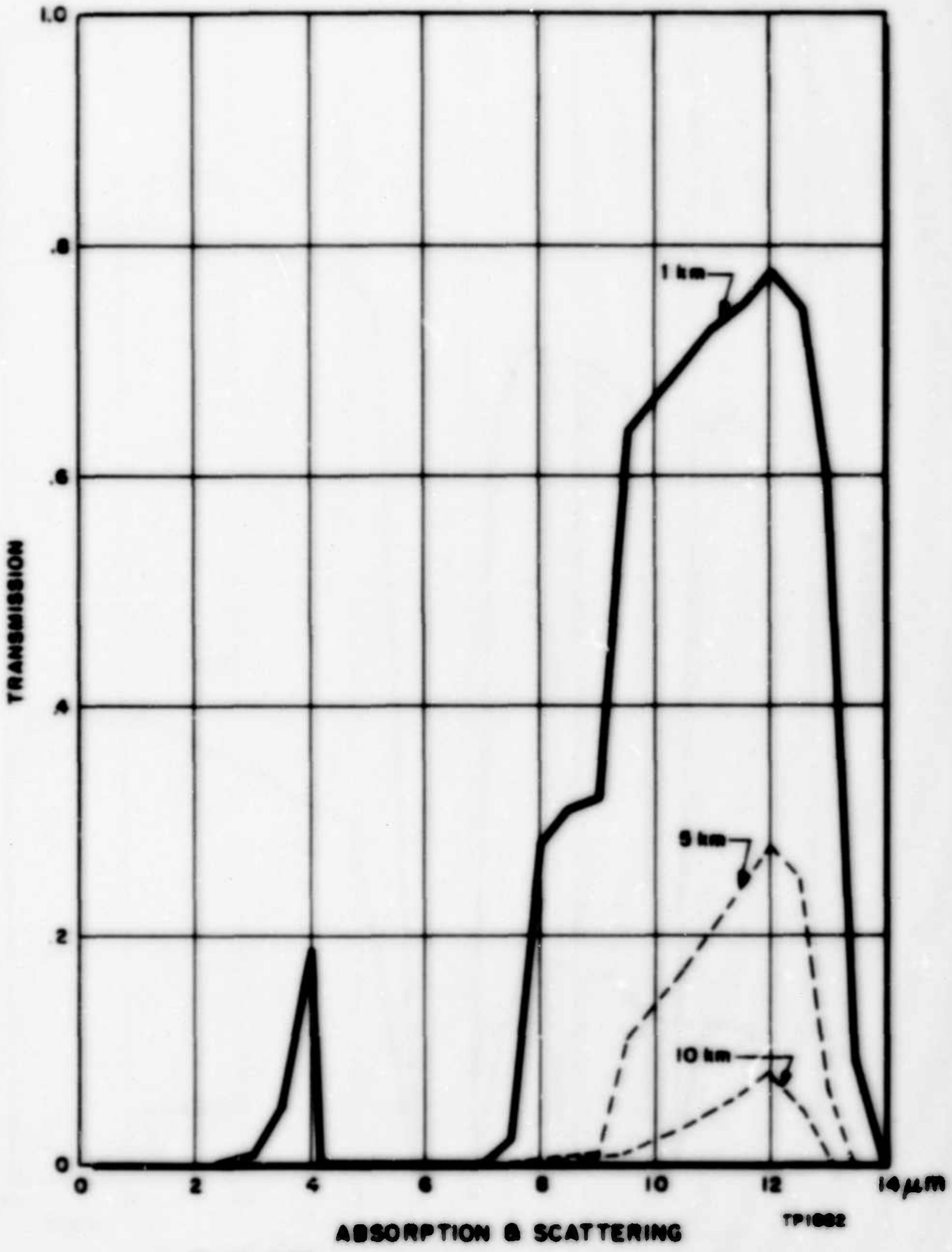


Figure 2-18. Spectral Transmission Through Light Fog

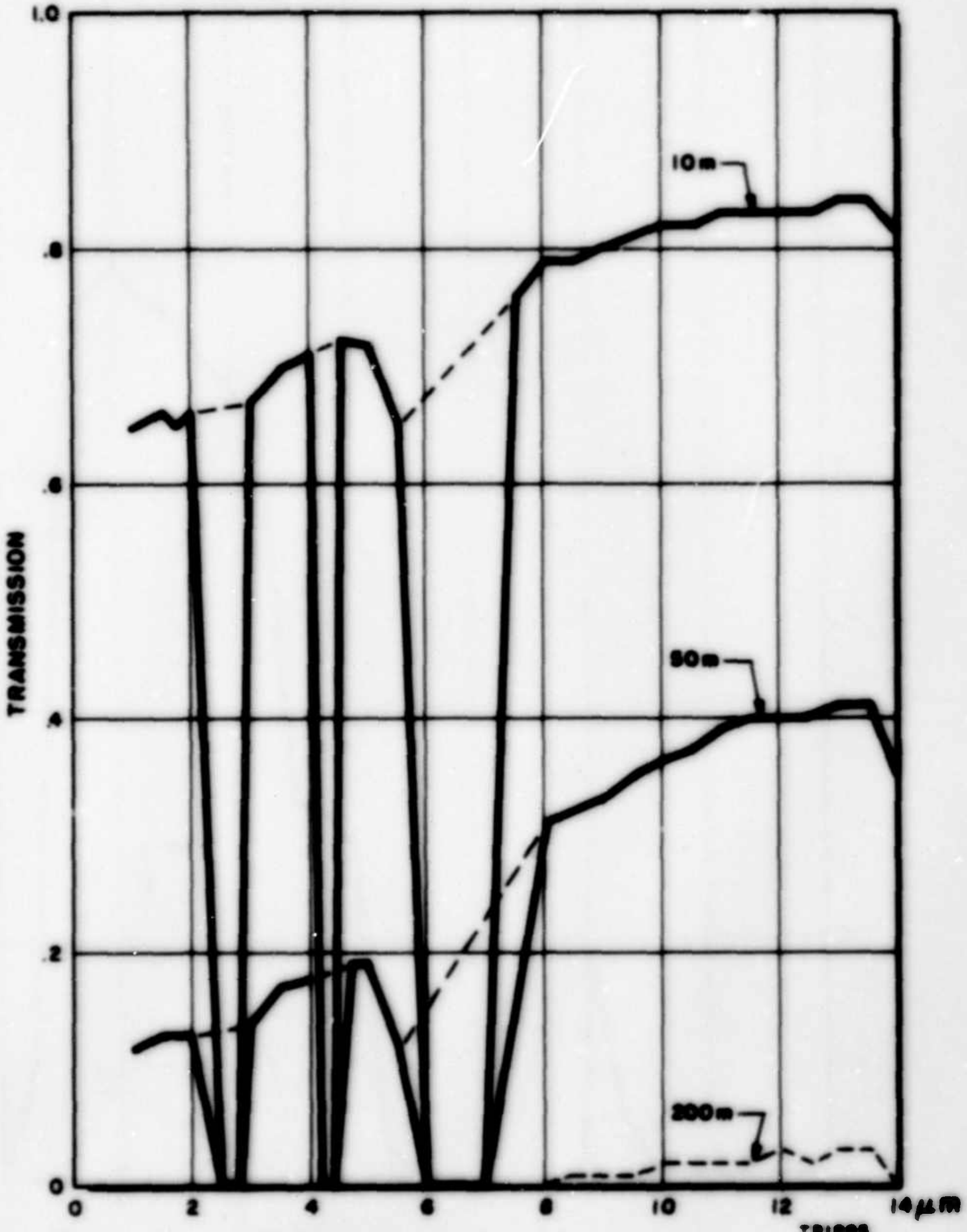


Figure 2-19. Spectral Transmission Through Medium Fog

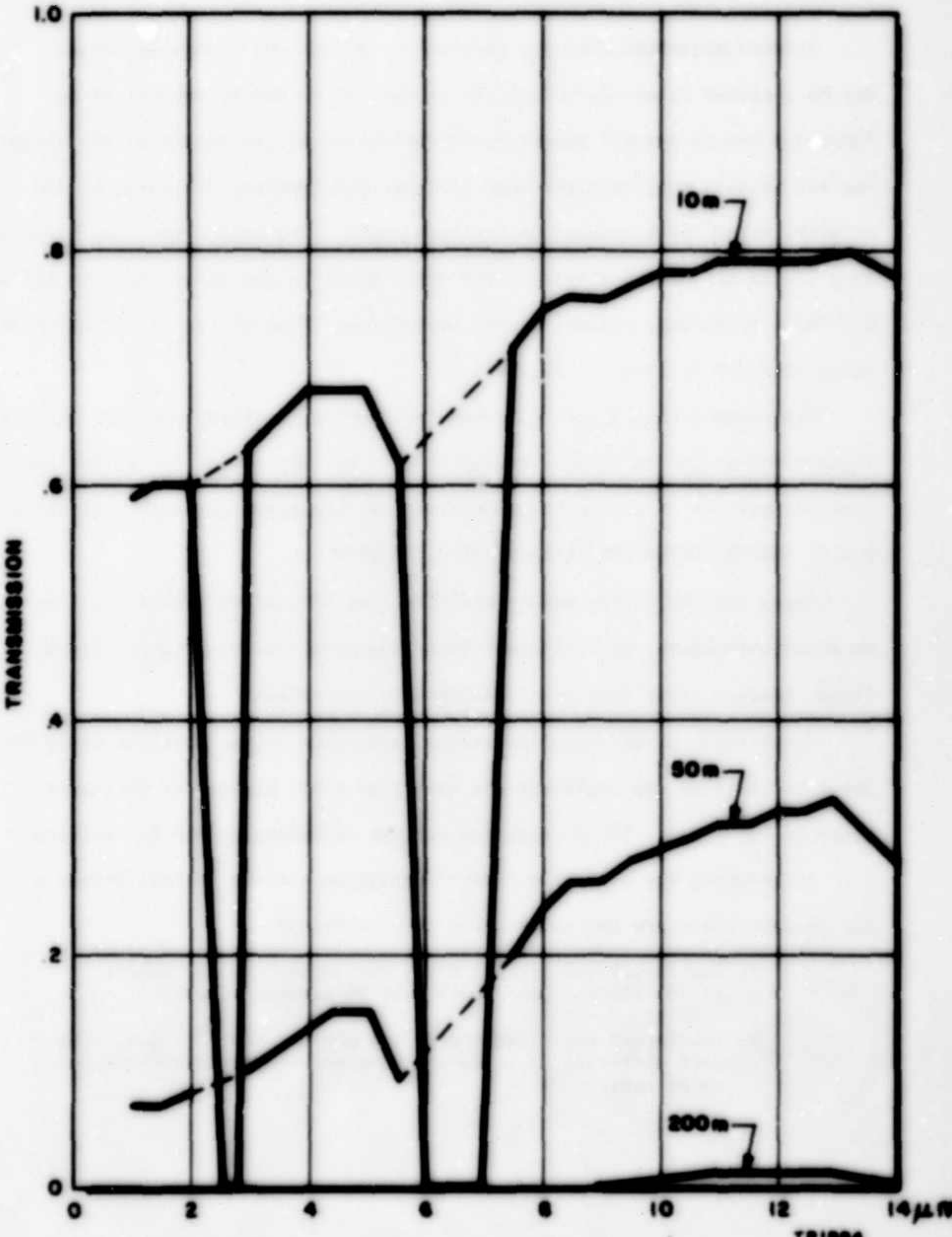


Figure 2-20. Spectral Transmission Through Heavy Fog

Johnson suggested that for purpose of perception, a complex target may be replaced by an equivalent bar pattern of frequency determined by Table 2-3 and an overall aspect ratio determined by the nature of the target. The bar pattern must have the same contrast and inherent S/N ratio as the original target with respect to its background. The sensor must now produce in a single bar at the display a S/N ratio equal to the value shown in Table 2-3 for a 50 percent probability of perception. Probability of detection vs. normalized S/N is shown in Figure 2-21.

Experiments have shown that when this procedure is followed for visible light systems, the calculated probability of perception for the target equivalent bar pattern is within 10 percent of that measured for the actual target.

2.4.5 SENSOR RESOLUTION REQIREMENTS - INFRARED

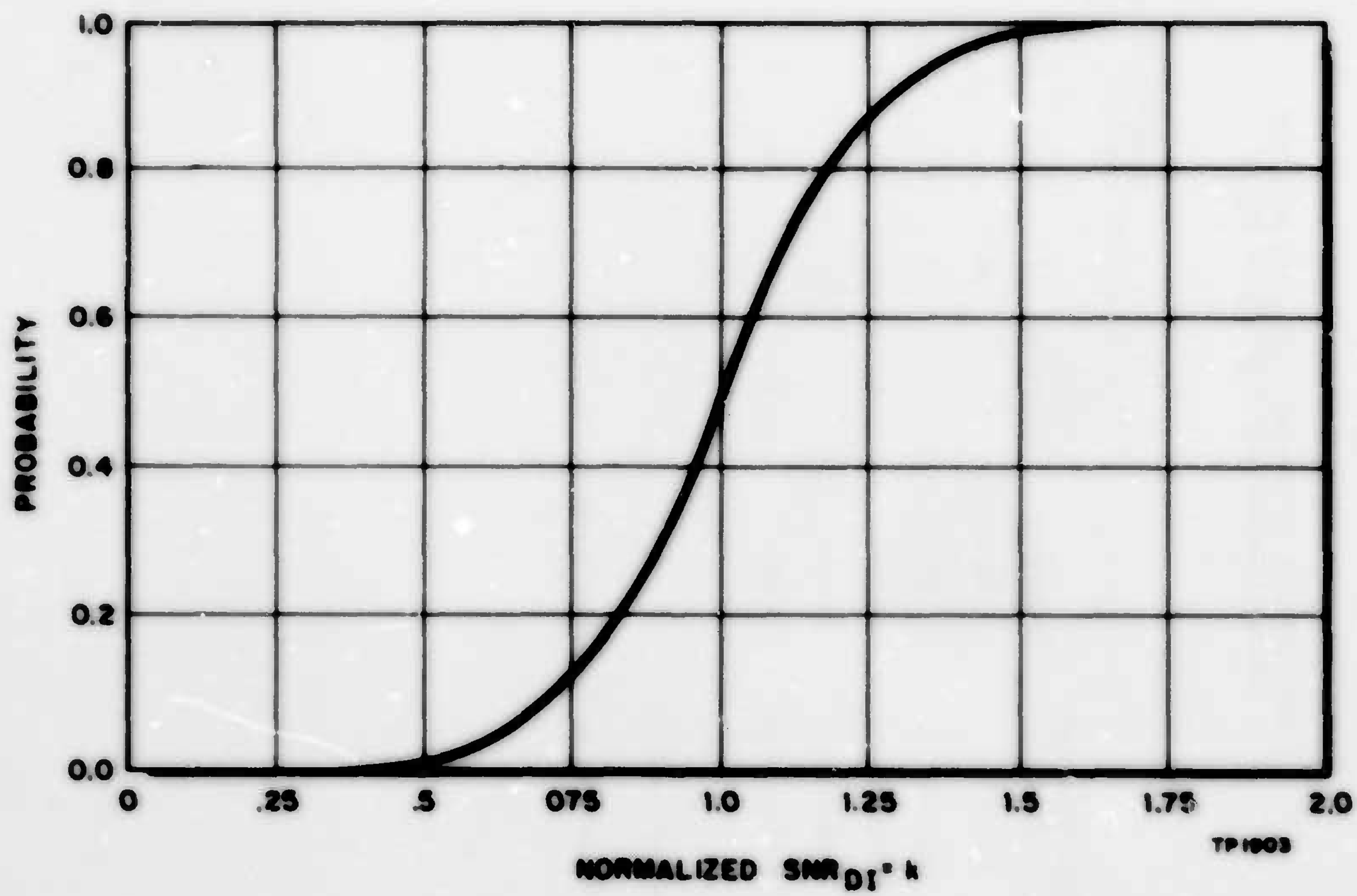
Since the resolution and sensitivity have historically characterized by seperate parameters, we will treat them seperately in this report, recognizing, however, that they are fundamentally equivalent.

An estimate of the required sensor resolution may be obtained using the Johnson criterion and replacing the target by a bar pattern of frequency given in Table 2-3. The problem now reduces to detecting the bar pattern.

In choosing the size of a sensor resolution element to best detect a bar pattern there are two conflicting considerations:

1. The larger the element size, the larger the throughput in the element when looking at an extended source.
2. The larger the element size the smaller the MTF, i.e., the more difficult it is to see contrast between the black and white bars.

Figure 2-21. Probability Vs. Normalized SNR_{DI}. For any Probability Value, obtain SNR_{DI} from Table 2.2-1 for 50% Probability. Find Value of k for desired Probability and Multiply Value of SNR_{DI} by k to obtain New Value of SNR_{DI} Required.



S72-0002-VA-46

TABLE 2-3

BEST ESTIMATE OF THRESHOLD SNR_{DI} FOR DETECTION, RECOGNITION AND IDENTIFICATION OF IMAGES

Discrimination Level	Background	k_d TV Lines per Minimum Dimension	Threshold SNR_{DI} for Spatial Frequency (Line/Pict. Ht.) of 100	300	500	700
Detection	Uniform*	1	←		2.8	→
Detection	Clutter	2	4.8	2.9	2.5	2.5
Recognition	Uniform	8	4.8	2.9	2.5	2.5
Recognition	Clutter	8	6.4	3.9	3.4	3.4
Identification	Uniform	13	5.8	3.6	3.0	3.0

*Treated as an Aperiodic Object.

It is shown in Appendix II that the optimum detector size for a perfect scanning system is the width of a black bar. The detector size at which the black and white bars are indistinguishable (MTF = 0) is the width of a black plus a white bar. The optimum resolution for an imperfect sensor is somewhere between these two limits. Figure 2-22 shows the optimum detector size for various targets as a function of range for both detection and recognition.

2.4.5.1 <u>Sensitivity Requirements</u>

It is assumed that the sensor must be able to provide the display S/N dictated by the Johnson criterion at the required spatial frequency as shown in Table 2-3.

Appendix I shows that the sensitivity required of a device to perceive a given target contrast or temperature difference at the scene is a function of atmospheric conditions and that the effect of atmosphere is to degrade temperature difference. Thus, if a temperature difference of 10°K exists between a target and its background and the atmospheric transmission between the target and sensor is 0.1, then the sensor must be able to detect a 1°K temperature difference. This approach is somewhat optimistic, since the analysis of Appendix I considers only energy losses from absorption and scattering. (As pointed out earlier, it does not consider that multiple scattering causes a blurring of a point source as well as energy loss and, therefore, a degradation in MTF.

Figure 2-23 to 2-26 shows the required sensitivity for an effective scene difference of 10°K as a function of atmospheric conditions and wavelength bands.

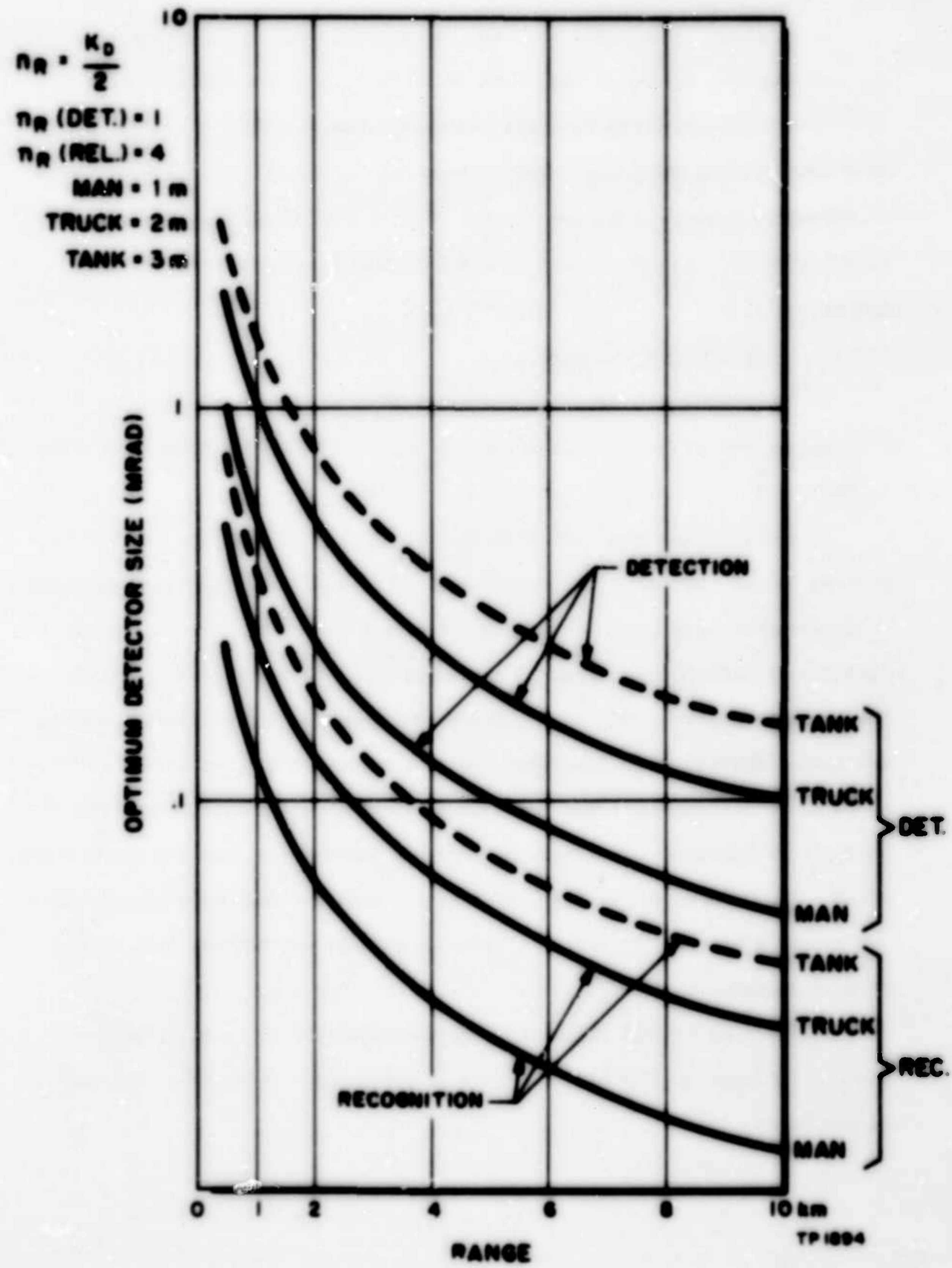


Figure 2-22. IFOV Requirements

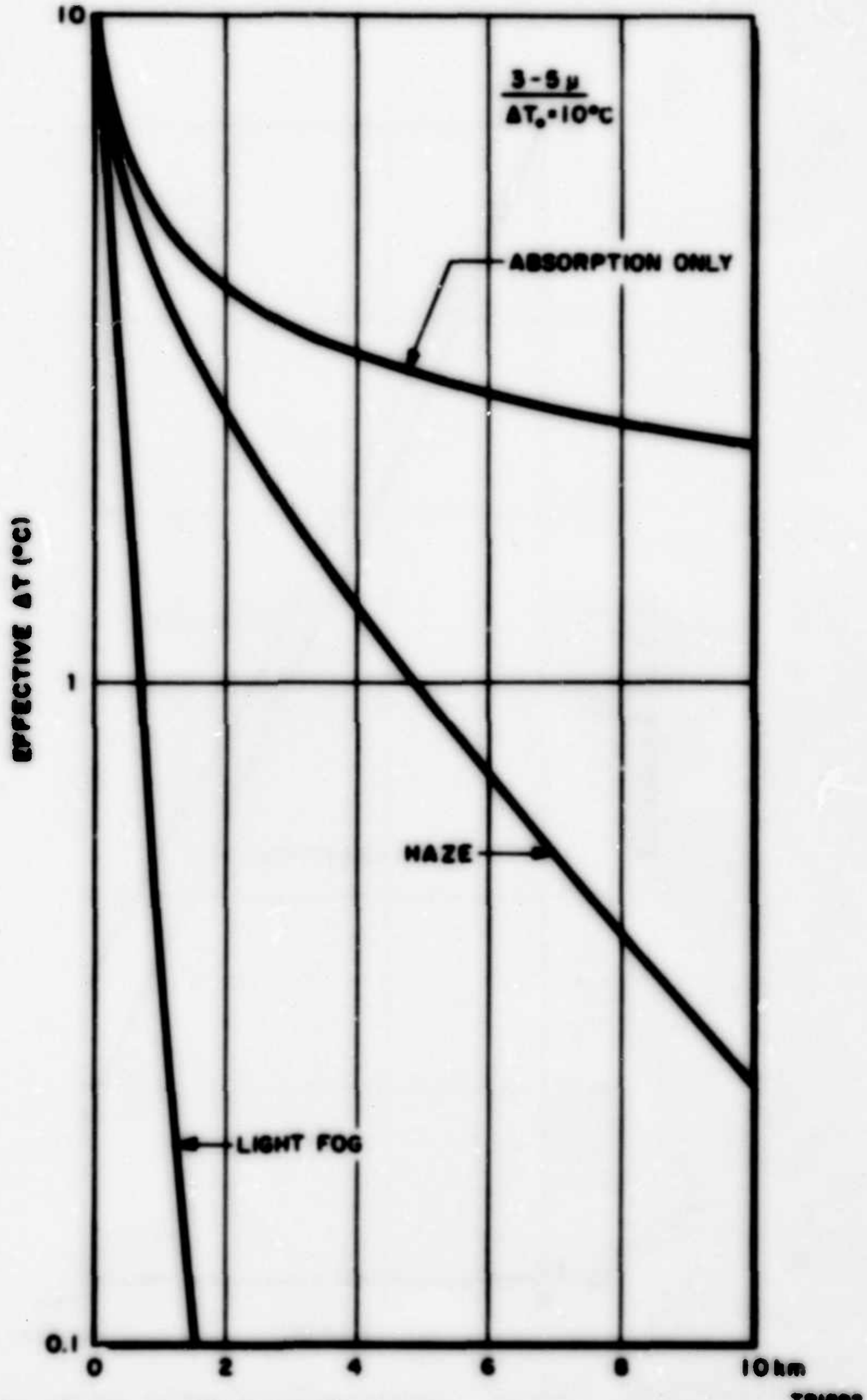


Figure 2-23. Range Vs. Effective ΔT for Clear Air, Haze and Light Fog - 3 - 5 um

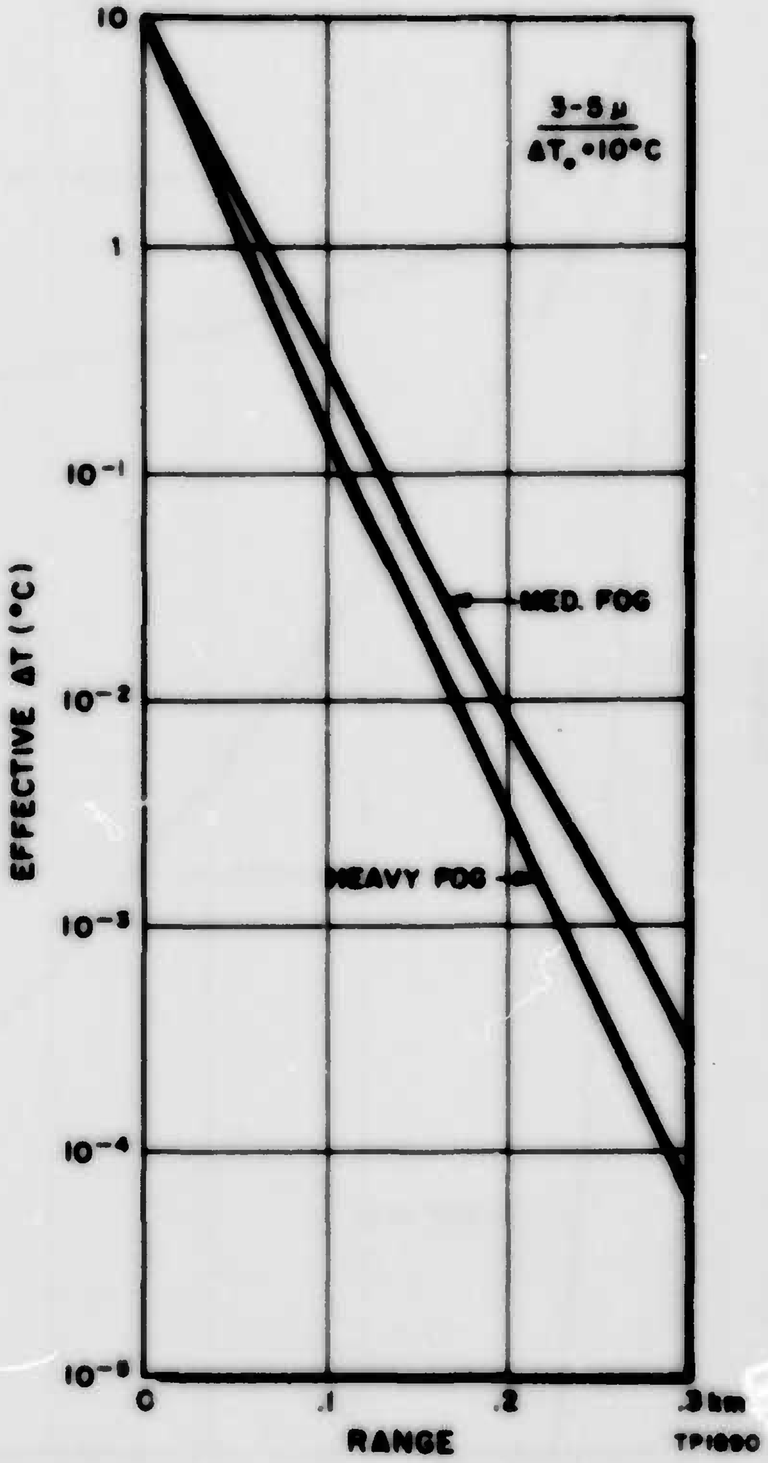


Figure 2-24. Range Vs. Effective ΔT for Medium and Heavy Fog - 3-5 μm

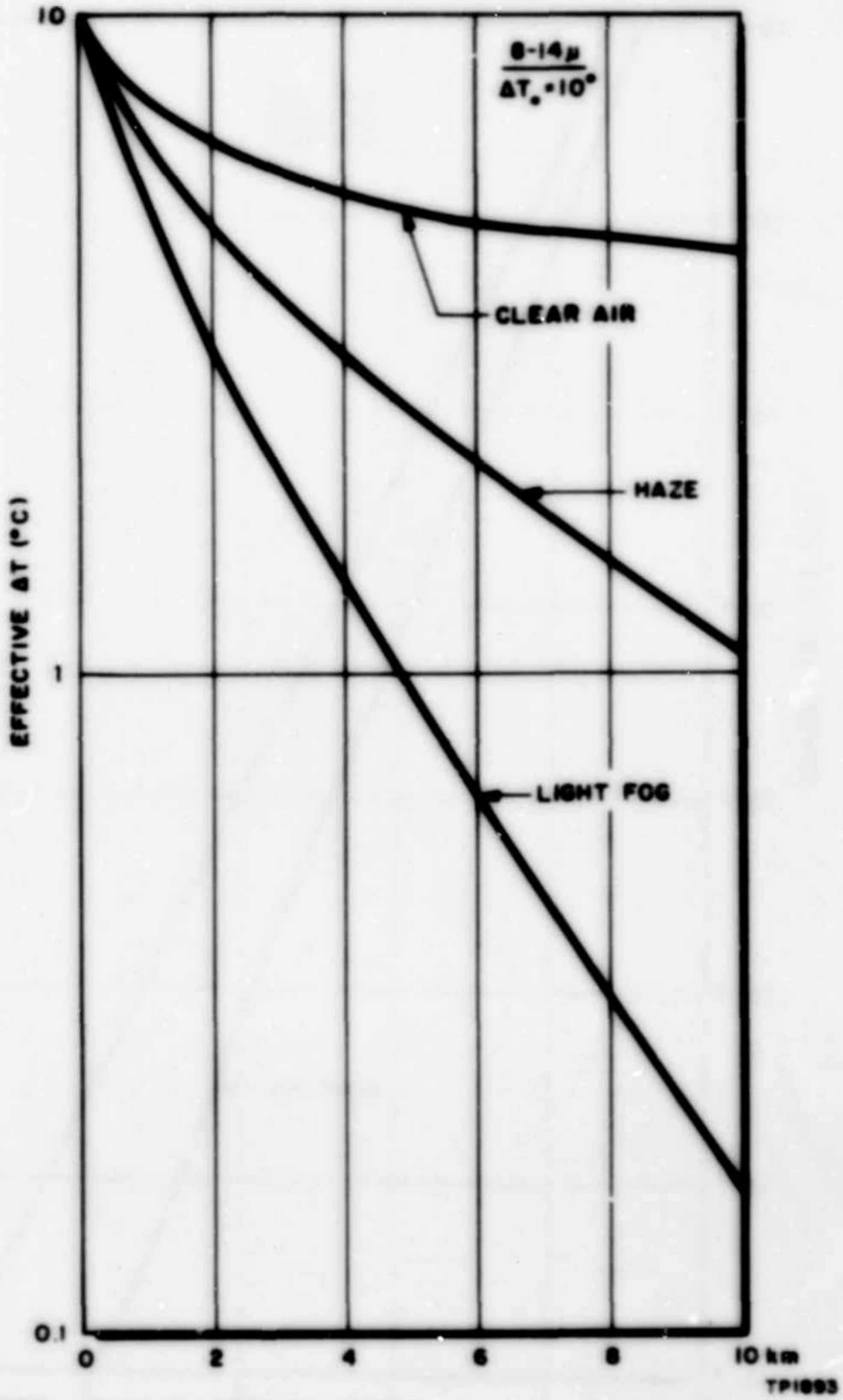


Figure 2-25. Range Vs. Effective ΔT for Clear Air, Haze and Light Fog - 8 - 14 μm

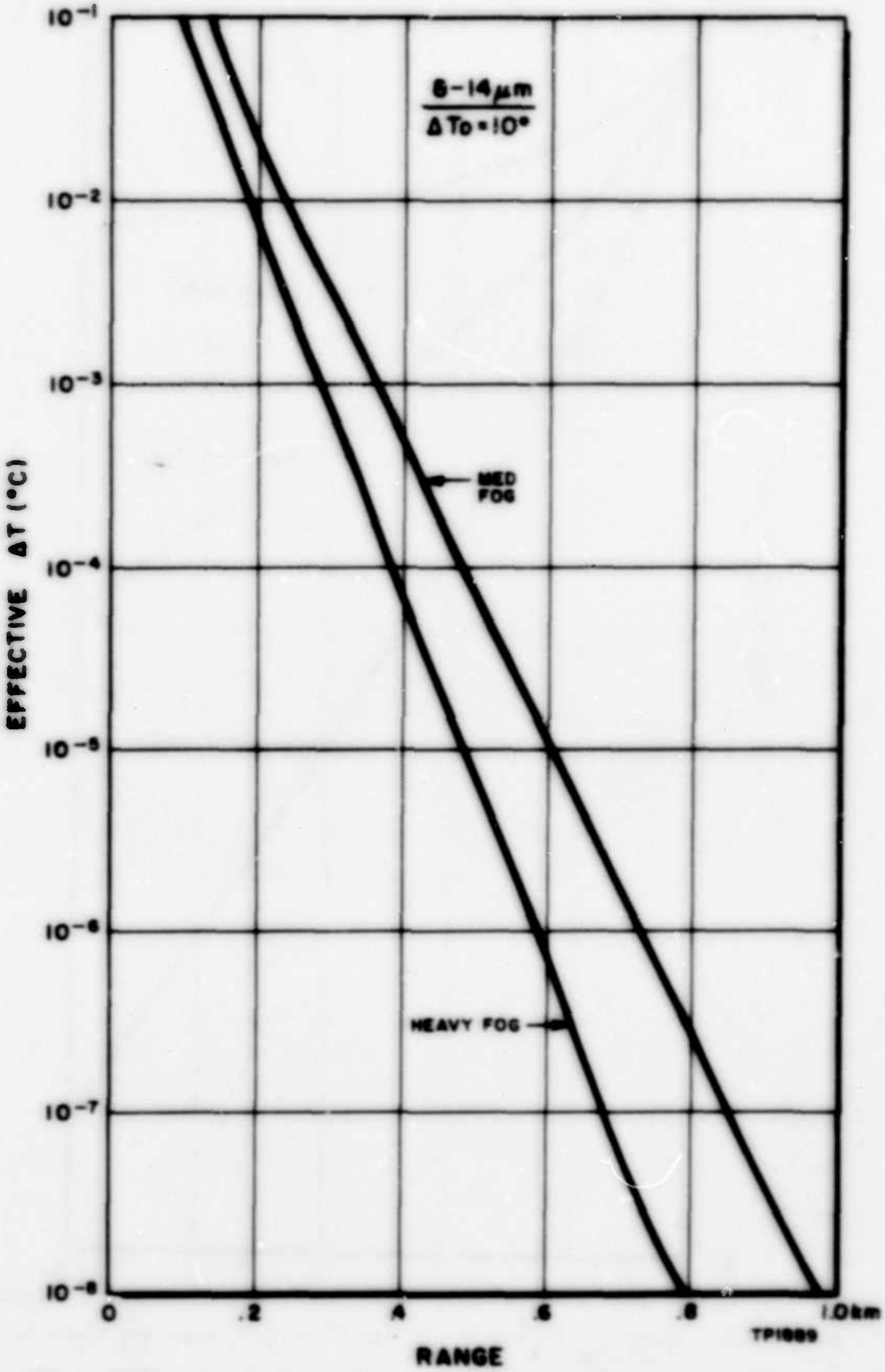


Figure 2-26. Range Vs. Effective ΔT for Medium and Heavy Fog - 8 - 14 μm

2.4.6 PERFORMANCE OF AN IDEAL SYSTEM

The performance of an ideal non-integrating passive system is derived in Appendix II and presented in Figures 2-27 - 2-33.

This formulation represents the ultimate performance of a single element sensor system optimized to perceive a target at a given range. It should be emphasized that the instantaneous FOV is optimized at each range as dictated in Appendix II, so that the curves showing performance as a function of range should not be interpreted as the performance achievable by a single system, but rather the locus of the best performance of optimized systems at each range.

Figure 2-27 shows the minimum effective scene temperature difference required for target recognition by a 3 - 5 micron system.

This system has a single element detector, 1° FOV, and 2 high collecting optics. The optical MTF is normalized to unity.

Figure 2-28 shows the performance of the corresponding 8 - 14 micron system, also ignoring MTF.

Figures 2-29, 2-30 and 2-31 prpvide multiplicative factors for the minimum resolvable temperature if one wishes to use a field of view or collecting optics other than 1° FOV, or 2 inches diameter, or more than a single detector, respectively. Figures 2-32 and 2-33 provide the information necessary to compute the optics MTF.

The T sensor is computed as follows:

$$T_{sensor} = T_{norm\ sensor} \times \frac{F_1 \quad F_2 \quad F_3}{MTF}$$

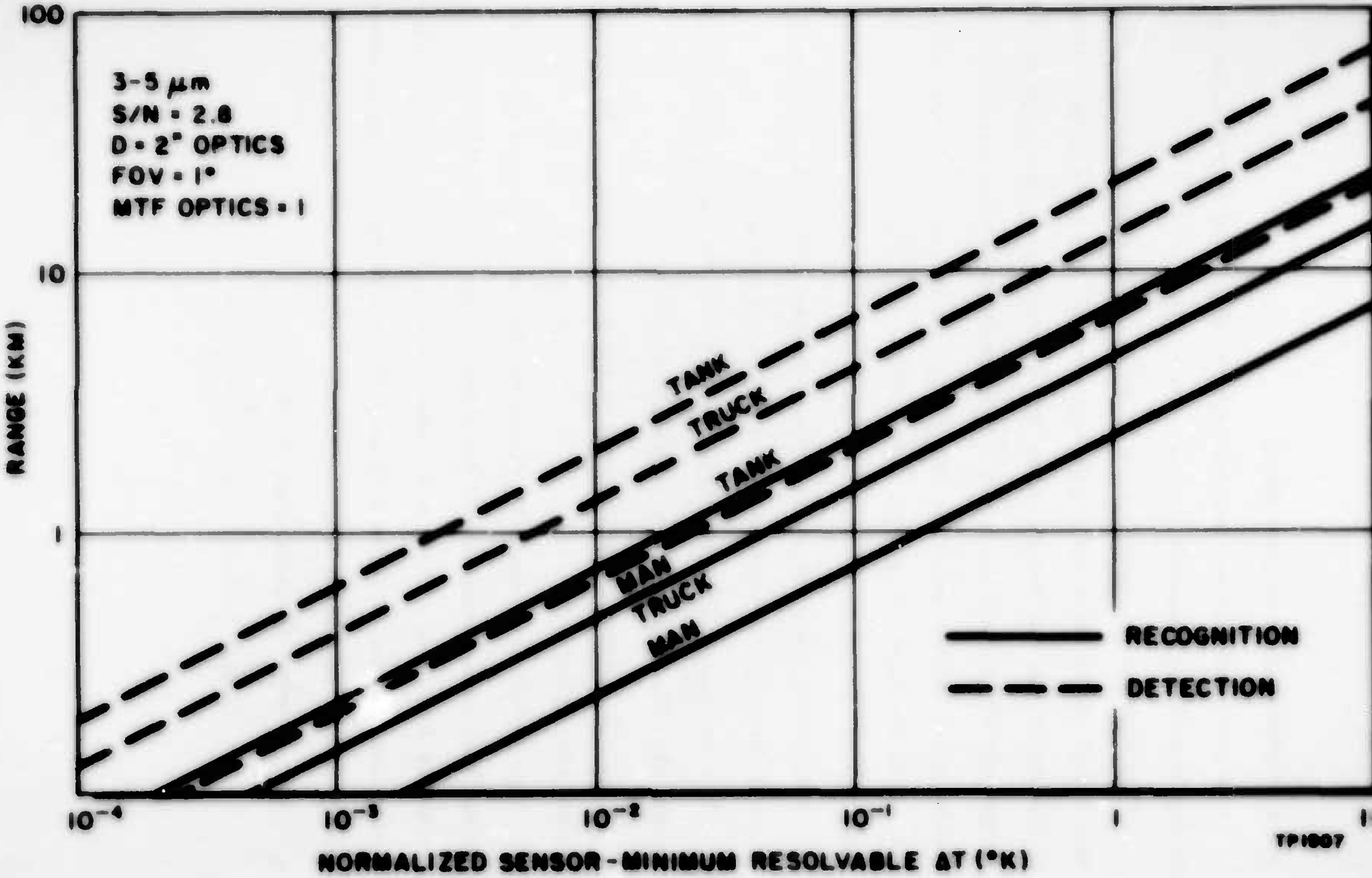

3-5 μm
S/N = 2.8
D = 2" OPTICS
FOV = 1°
MTF OPTICS = 1
TANK
TRUCK
TANK
MAN
TRUCK
MAN
RECOGNITION
DETECTION
100
10
1
RANGE (KM)
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
10
TP1007
NORMALIZED SENSOR-MINIMUM RESOLVABLE ΔT (°K)

Figure 2-27

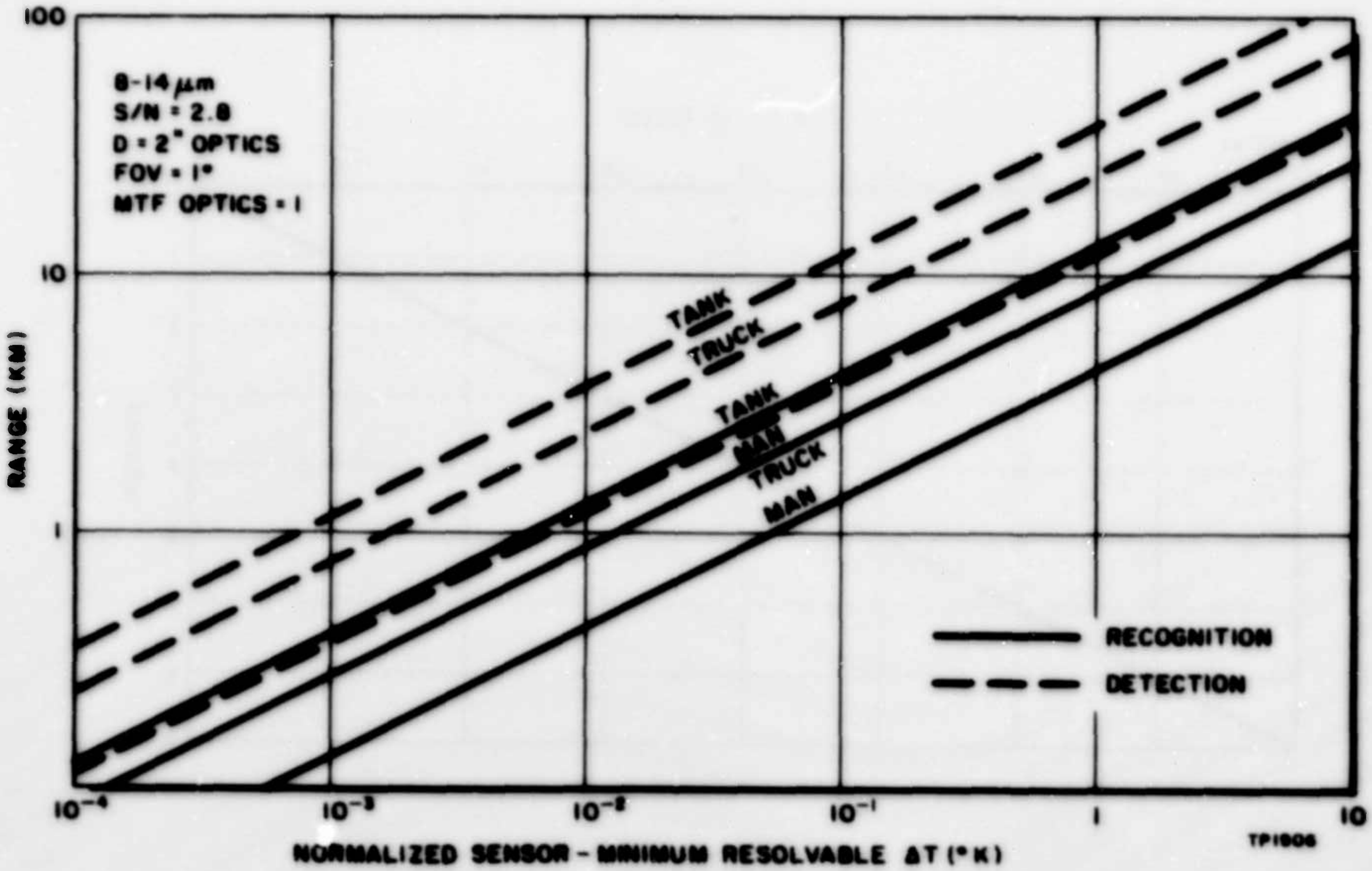

8-14 μm
S/N = 2.8
D = 2" OPTICS
FOV = 1°
MTF OPTICS = 1
RANGE (KM)
100
10
1
TANK
TRUCK
TANK
MAN
TRUCK
MAN
RECOGNITION
DETECTION
10⁻⁴
10⁻³
10⁻²
10⁻¹
1
10
TP1906
NORMALIZED SENSOR - MINIMUM RESOLVABLE ΔT (°K)

Figure 2-28

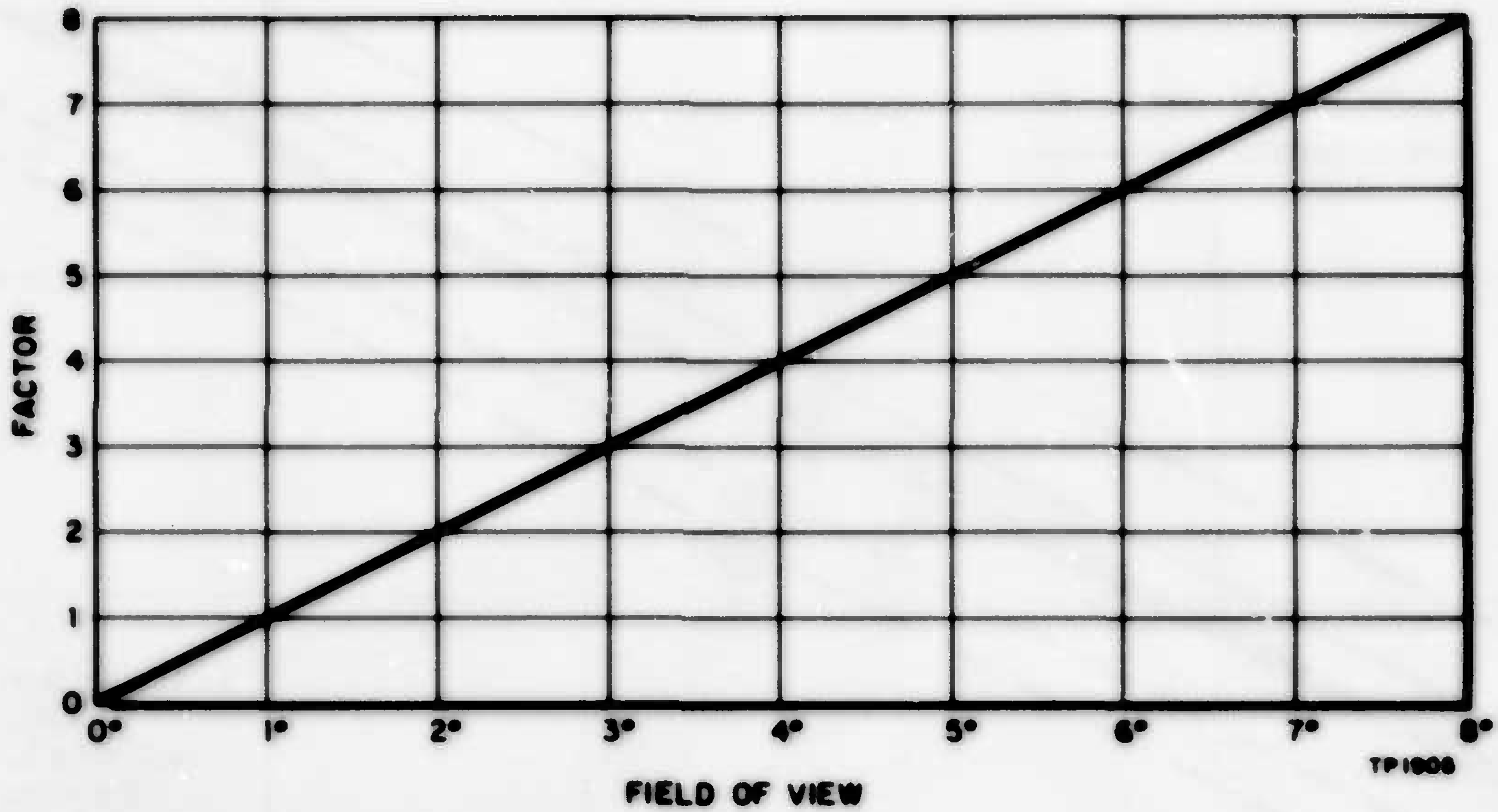


Figure 2-29. Multiplication Factor for Field of View

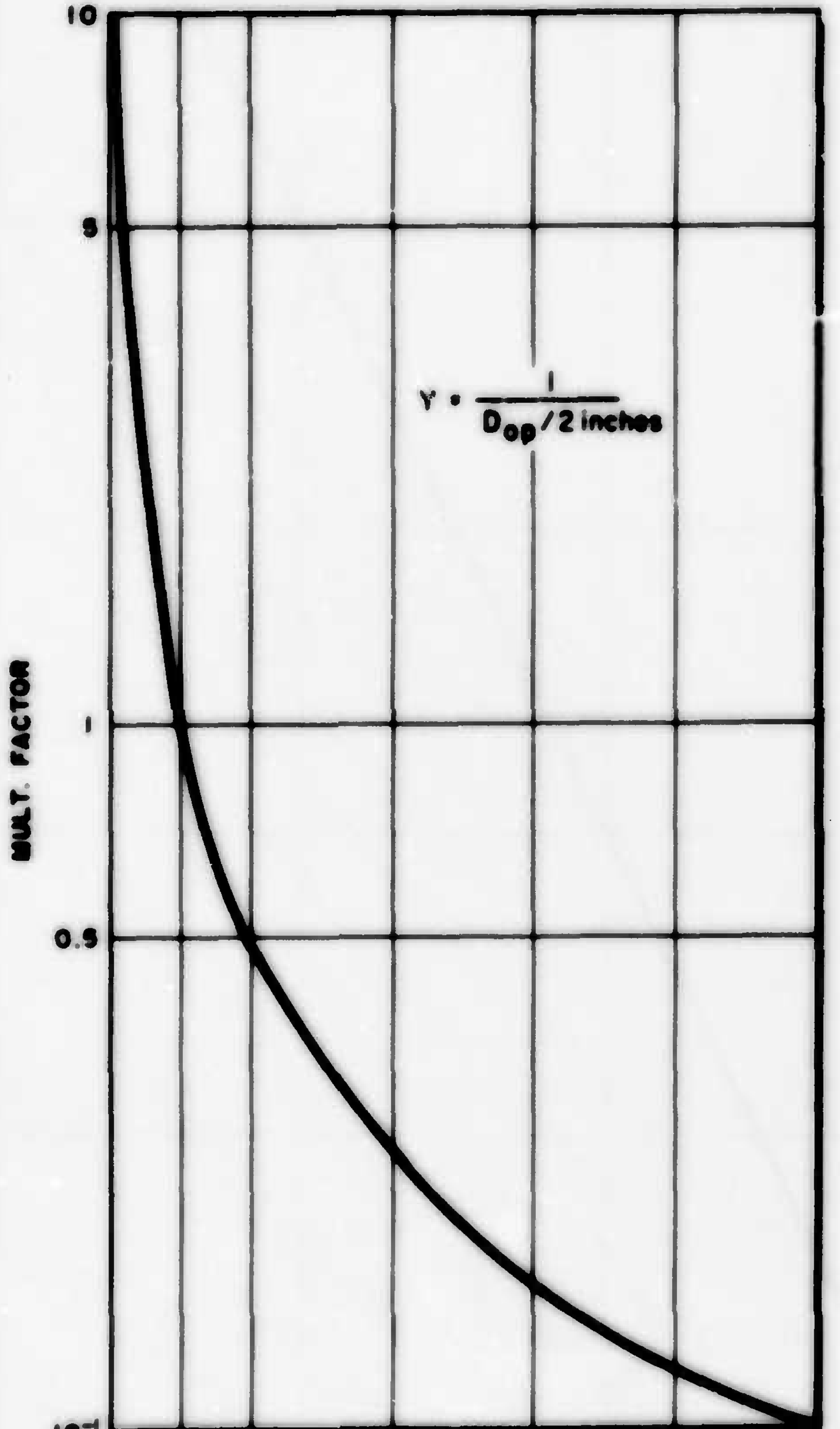


Figure 2-30. Multiplication Factor for Optics

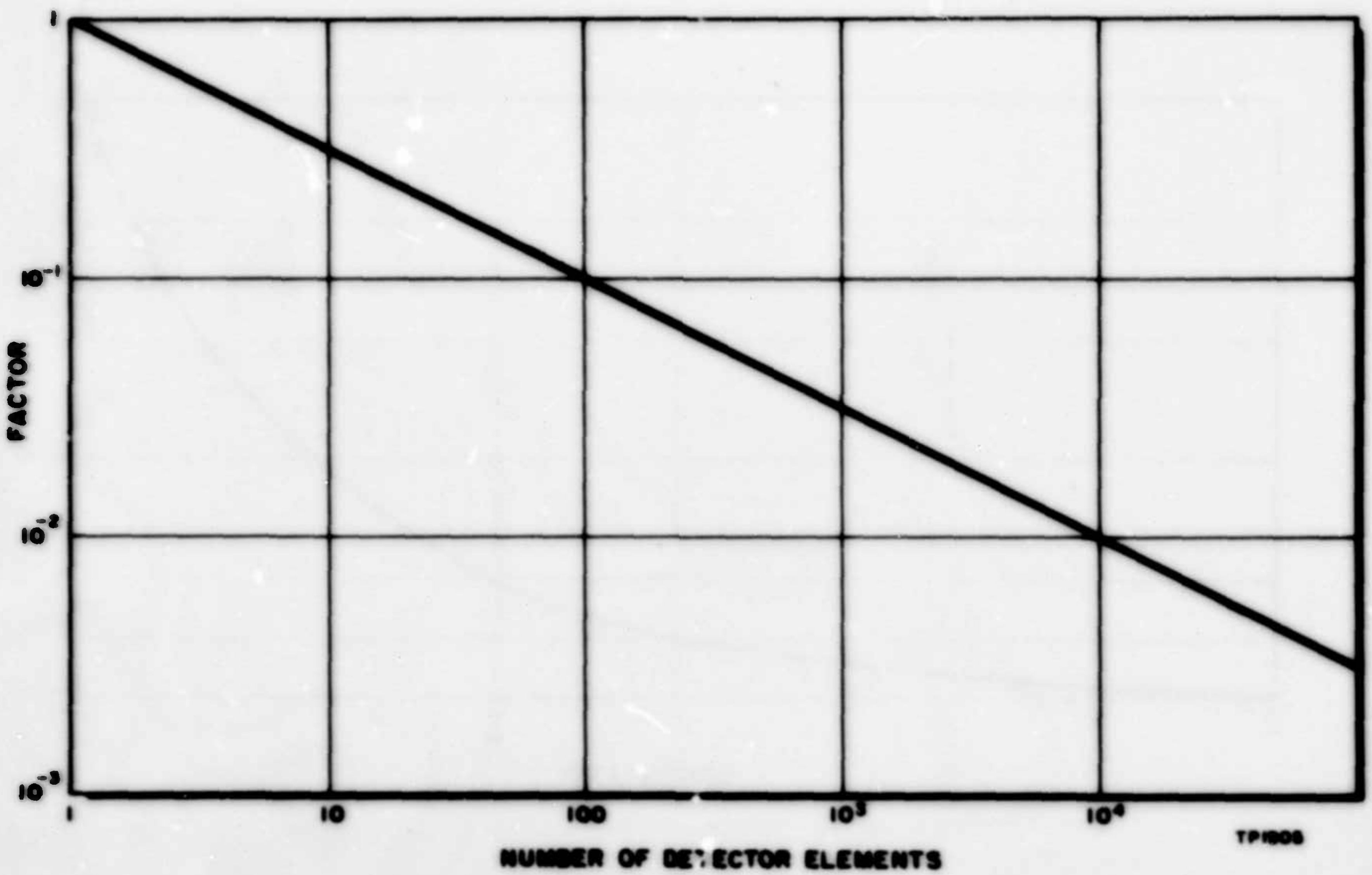


Figure 2-31. Multiplication Factor for Multi-element Detectors

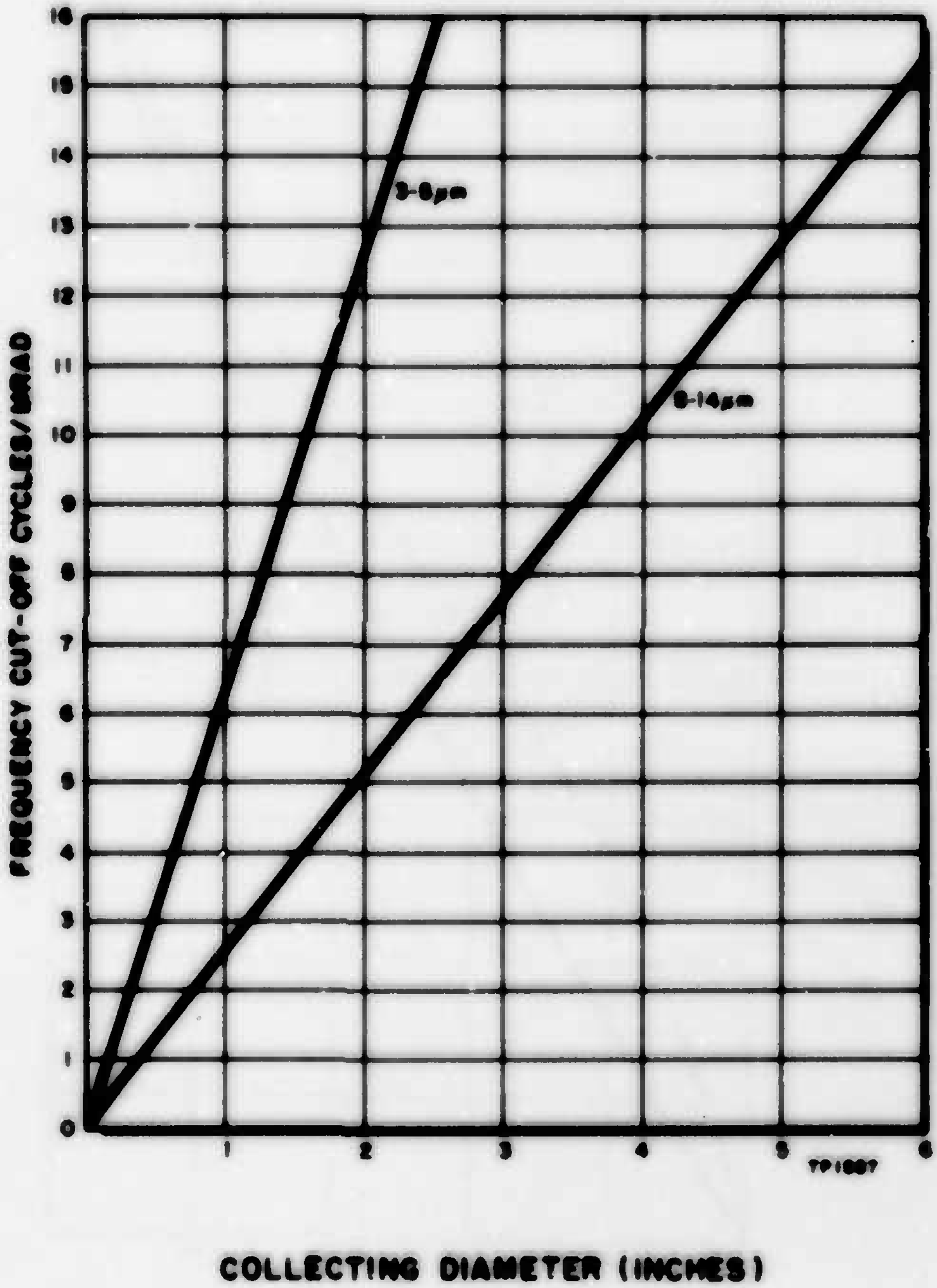


Figure 2-32. Optical Cut-off Frequency for the 3 - 5 μm and 8 - 14 μm Regions as a Function of Collecting Diameter

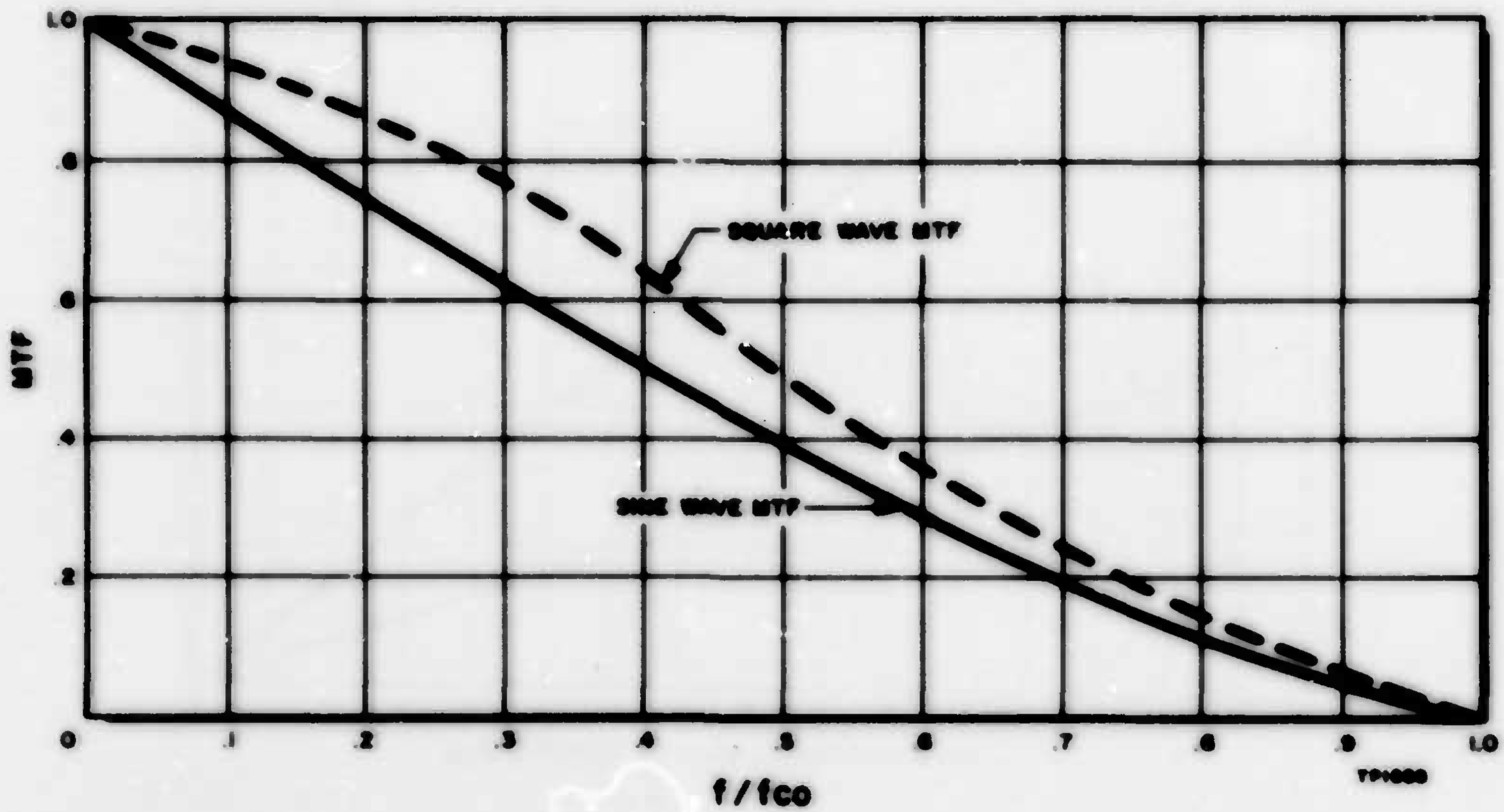


Figure 2-33. Optical Modulation Transfer Function

where:

$\Delta T_{norm\ sensor}$	→	This is the minimum ΔT obtained from the normalized sensor (see Figure 2-27 or 2-28)
F_1	→	factor that accounts for field of view (see Figure 2-29
F_2	→	factor that accounts for optics diameter (see Figure 2-30)
F_3	→	factor that accounts number of detected elements (see Figure 2-32)
MTF	→	Modulation Transfer Function of Optics (see Figure 2-32 and Figure 2-33)

2.5 PHASE SHIFT CORRECTION AND RESIDUAL PHASE SHIFT MTF

2.5.1 GENERAL

Back and forth scan systems with interlace are prone to display vertical lines with stagger if some form of phase shift correction is not employed. It can be shown that the effect of a phase shift ϕ in the channel amplifiers is to degrade the system MTF by a factor cos (ϕ). Clearly, it is desirable to make ϕ as small as possible over the entire spatial frequency range of an imaging system. One method of doing this is to make use of the fact that the phase shift produced by an amplifier is roughly proportional to the frequency.

For a signal input to the channel amplifiers of sin (ωx) the output will be sin$(\omega x - \phi)$. This may also be written as

$$\sin \left[\omega(x - x(\omega)) \right]$$

where $x(\omega)$, the apparent displacement for spatial frequency ω is given by

$$x(\omega) = \phi/\omega.$$

If ϕ were precisely proportional to the frequency, then $x(\omega)$ would be independent of the frequency and the image would appear sharp but displaced. It would have opposite displacement for the other scan direction and, for interlaced systems like those built with common modules, would produce a staggered

vertical image from a straight vertical object. This image would appear wider to an MTF measuring device, and this is what causes the system MTF to be degrade `y the cosine factor.

Phase shift can be corrected by introducing displacements into the display device which will bring the images of the two interlaced fields back into line. In the common modules system this is done by means of a lens in the interlace gimbal placed so that it moves very slightly from side to side, displacing the image in different directions depending on which interlace is being scanned.

In reality, ϕ is an arc tangent function of frequency and not exactly proportional to ω. Also, there are variations between detectors and amplifiers, which change the amount of phase shift, and hence apparent displacement, between channels. The phase shift lens can produce only one displacement for all frequencies and channels, so the magnitude of this correction should be chosen to produce a sort of median displacement, thus minimizing the differences to each extreme.

The apparent displacements due to two channels, one at each limit of high-cut frequency tolerance and each coupled to detectors of different time constants, represent the worst case limits.

The MTF due to the phase shift after correction is then

$$T_{ps}\,(\omega) = \cos\,(\phi - \omega x_e)$$

where x_e is the displacement produced by the phase shift lens for one interlace (or half the peak-to-peak displacement between interlaces).

2.5.2 AVERAGE VS. WORST CASE PHASE SHIFTS

An MTF or MRT measurement involves several channels, not all (or not any) of which may be worst case channels.

We may assume that the effective phase shift will fall closer to the nominal phase shift than the worst case tolerance values. Assume the average toleranc as being some factor γ times the maximum. Now, one must establish the value of γ which would represent a real situation as far as the distribution of pole frequencies is concerned. If we assume that the distribution of frequencies is Gaussian and that 95 percent of the area under the Gaussian falls within the tolerances on the frequencies, then 50 percent of the area under the curve is contained between limits which are approximately one-third of these tolerances. The residual phase shift MTF will be calculated for hi-cut frequency limits which are one half the specified tolerance limits ($\gamma = 0.5$). The detector time constant limits will be taken to be one and four microseconds. The larger of the average residual apparent displacements will be converted to phase shift and used as the argument of the MTF cosine factor when calculating system MTF. Table 2-4 gives the resultant hi-cut frequencies in kHz and equivalent spatial frequencies for a 30 frame/sec scan rate.

TABLE 2-4

TYPICAL "AVERAGE" ELECTRONIC HIGH-CUT FREQUENCIES
WHICH DETERMINE RESIDUAL PHASE SHIFT MTF-SCAN RATE = 30 FRAMES/SEC

	Hi Phase Shift Channel		Nominal Channel		Lo Phase Shift Channel	
	(kHz)	(cycles/mr)	(kHz)	(cycles/mr)	(kHz)	(cycles/mr)
Detector	39.8	10.7	63.6	17.2	159	43
Preamp	92.5	25	105	28.4	117.5	31.8
Post Amp	90	24.4	110	29.8	130	35

The apparent displacements due to phase shift in these channels are plotted in Figure 2-34 along with worst case high and low displacements and the displacement for a nominal channel coupled to a 2.5 microsecond detector.

The horizontal line at 0.125 x DAS is the displacement selected to be removed by the phase shift lens. No apparent displacement for any channel is more than 0.25 x DAS away from this correction line. As another advantage, this amount of correction tends to make the worst case displacements approximately equal for high MRT spatial frequencies. This means that the back scan and the forth scan will be in register for this frequency, which is likely to be the most critical when measuring MRT.

Figure 2-35 is a plot of the MTF caused by the residual phase shift, the difference between the apparent displacement caused by the residual phase shift lens and the displacement of an average channel. This has been approximated by the phase shift equivalent of a constant displacement independent of frequency (0.45 *DAS). This leads to a residual phase shift MTF of

$$T(f) = \cos(2\pi f (0.45 * DAS))$$

where f is now an object space frequency.

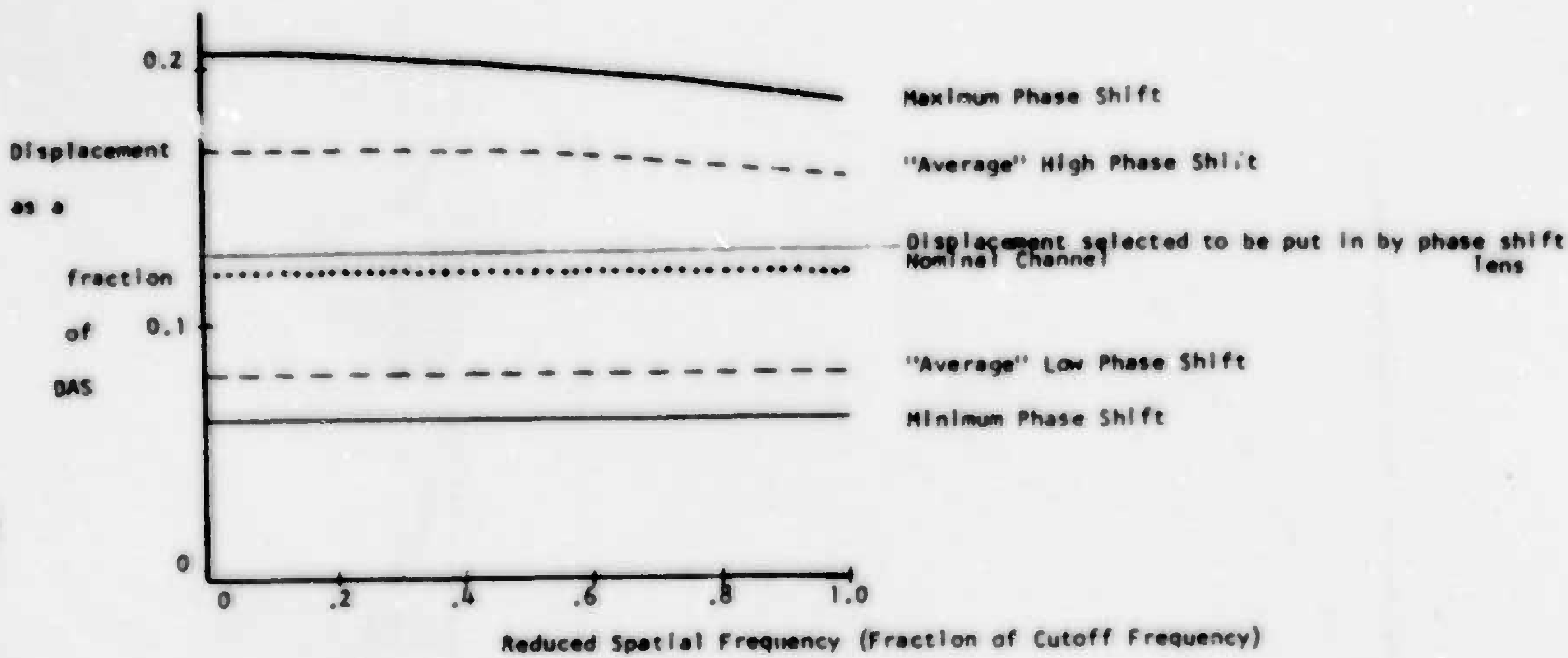


Figure 2-34. Displacement Due to Phase Shift Vs. Spatial Frequency for a 30 Frames/Sec System. Phase Shift Lens Correction = 0.125 x Detector Angular Subtense (DAS)

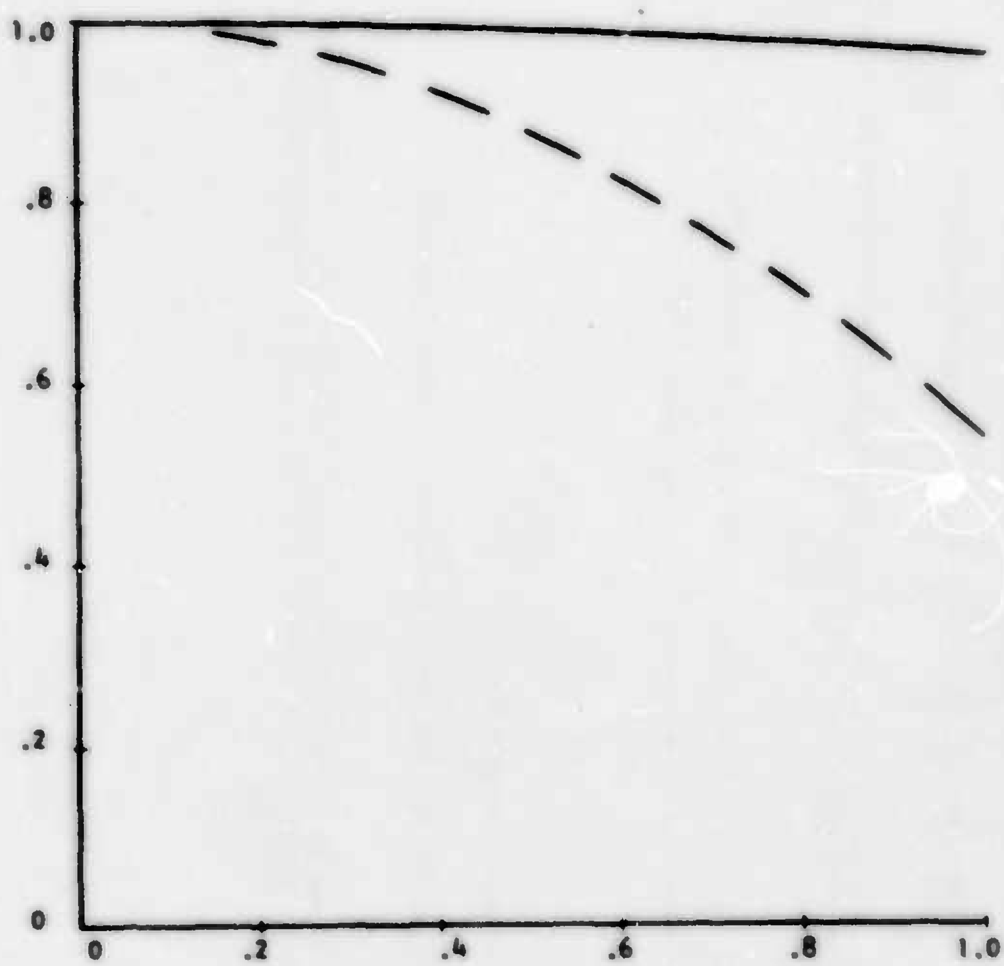


Figure 2-35. MTF Caused by Residual Phase Shift Vs. Reduced Spatial Frequency. Dashed line shows approximate MTF due to phase shift if no phase shift correction is used.

2.5.3 PHASE SHIFT LENS CONSIDERATIONS

Figure 2-36 is a simplified drawing of the mechanical scanner. The mechanical scanner serves a dual purpose; scan of the IR beam on one side of the mirror, and synchronized scan of the visible display via the opposite surface of the mirror. The scanner has two gimbal axes, the azimuth scan axis and the elevation interlace axis. Since the scan mirror motion is back and forth in azimuth, time delays in the signal processing electronics (phase shift) will mis-register the images scanned in opposite directions. Incorporation of a phase shift lens in the visible optical path corrects this shift. In effect, motion of the phase shift lens produces an optical shift of correct magnitude to produce registry of the images when scanned in both directions.

The phase shift lens is mounted on the elevation interlace gimbal. As can be seen by Figure 2-36(b) θ rotation of the elevation interlace gimbal can be resolved into motions α and β, which correspond to azimuth and elevation respectively. The motion of the phase shift lens in azimuth can be expressed as $r\alpha$. Since all other optical lenses in the visible optical train are fixed, $r\alpha$ motion of the lens produces an optical shift in azimuth. The magnitude naturally depends upon the parameters as shown in Figure 2-36(B), distance r, and focal length of the phase shift lens. Varying the focal length of the phase shift lens can accommodate any desired combination of scan rate and scan angle.

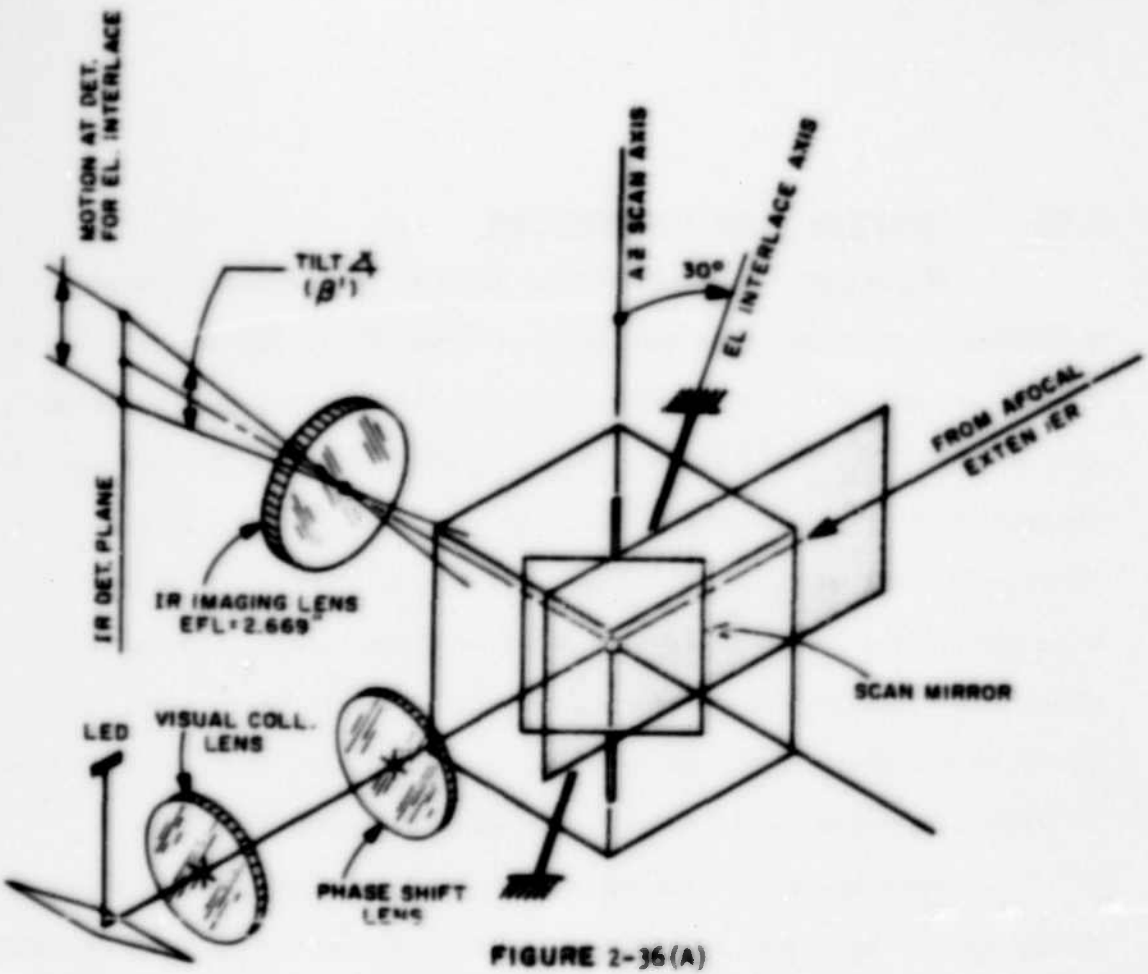


FIGURE 2-36(A)

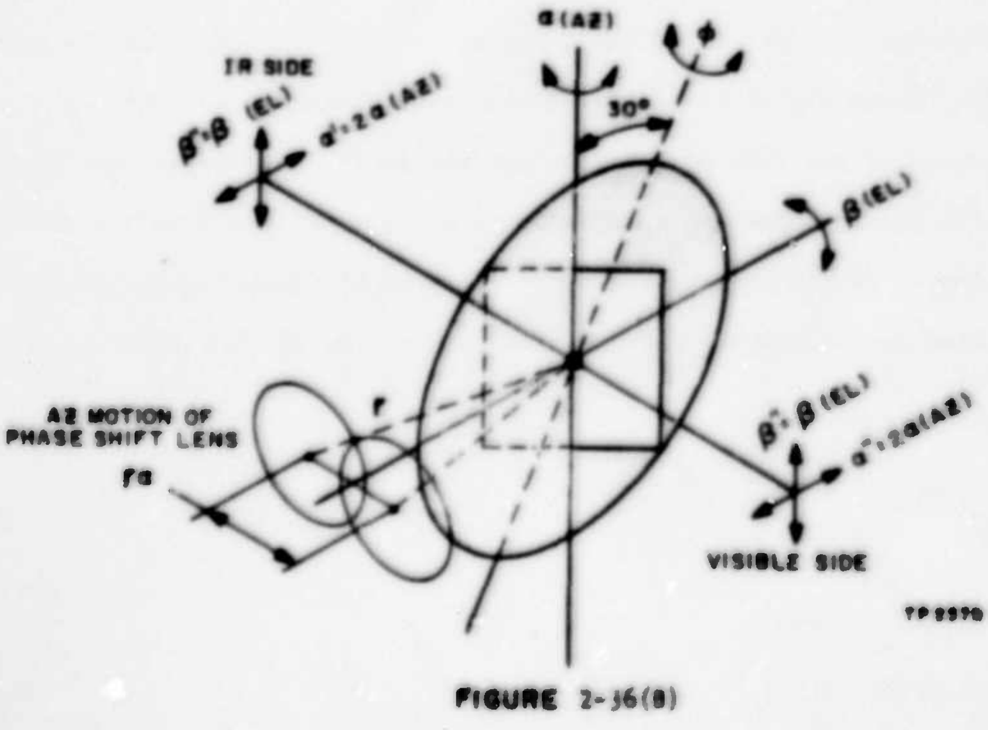


FIGURE 2-36(B)

The elevation motion is determined by the interlace requirements of the IR detector array.

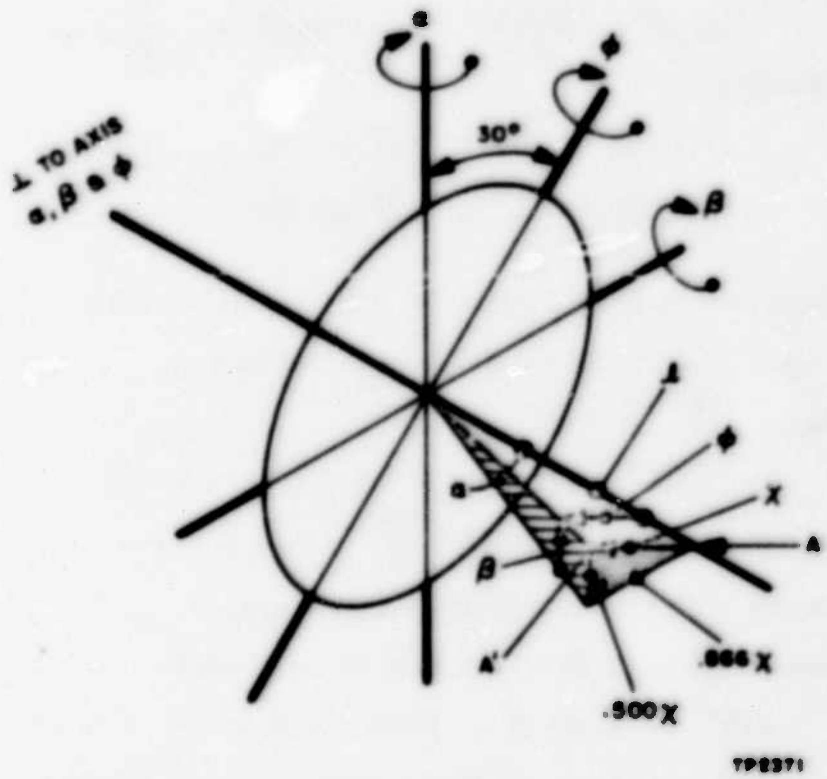


Figure 2-37

RELATIONSHIP OF α TO β TO ϕ. See Figure 2-37

Consider a small rotation of the line about ϕ, moving point A to A', a distance X

Then: $\tan\phi = \frac{1.00\,X}{\ell}$ or $1.00\,\phi = \frac{X}{\ell}$

$\tan\alpha = \frac{.866\,X}{\ell}$ or $1.55\,\alpha = \frac{X}{\ell}$

$\tan\beta = \frac{.500\,X}{\ell}$ or $2.00\,\beta = \frac{X}{\ell}$

Equating:

$$1.155\,\alpha = \frac{X}{\ell} = 2\beta \text{ or } \alpha = 1.732\beta$$

$$1.00\,\phi = \frac{X}{\ell} = 2\beta \text{ or } \phi = 2.00\beta$$

Referring to Figure 2-36 the relationship of image motion on both IR side and visible side is 1:1 with β and 2:1 with α.

Hence: $\phi = 2\beta' = 2\beta$

$*\alpha'' = 2\alpha = 2 \times 1.732\,\beta = 3.464\,\beta$

We know from Figure 2-36(A) $\beta' = 0.75$ mr

Assume r in Figure 2-36(B) = 1.200 inch.

Hence: $\phi = 2\beta = 2 \times 0.75$ mr $= 1.50$ mr

$*\alpha'' = 3.464\,\beta = 3.464 \times 0.75$ mr $= 2.60$ mr

$r\alpha = 1.2 \times 1.732 \times 0.00075/\text{inch} = 0.00156''$

Figures 2-38, 2-39 and 2-40 graphically illustrate the principle of operation of the phase shift lens. Since it is located in the collimated beam, a

*It should be noted that in actual operation α'' is cancelled by an equal and opposite motion α'. See Figure 2-36.

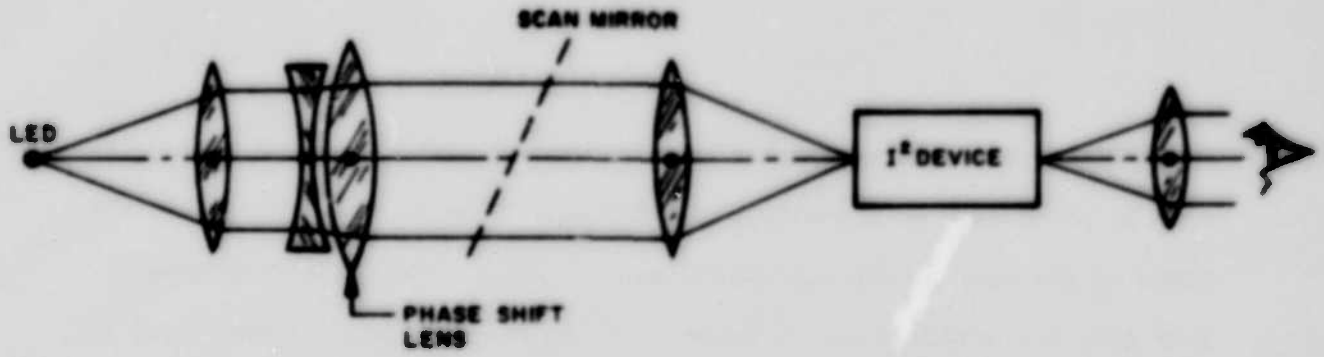


FIGURE 2-38

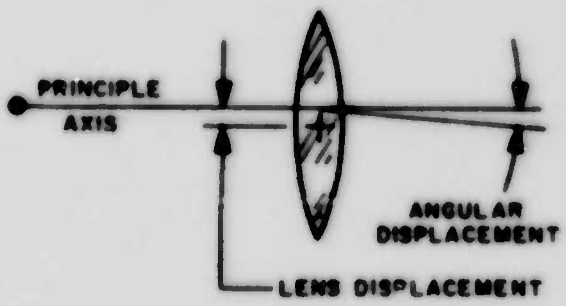


FIGURE 2-39

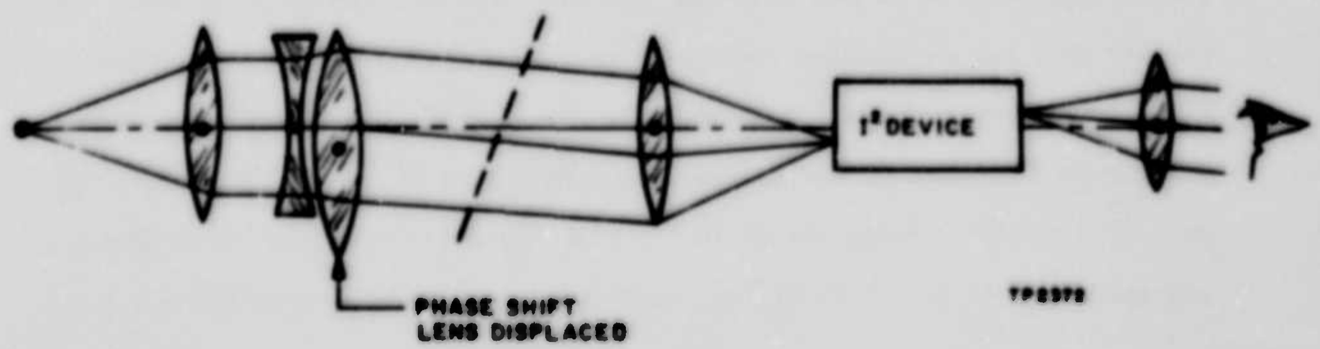


FIGURE 2-40

displacement produces an angular displacement of the collimated beam. It will be noted that an opposite and equal power lens is used to nullify the power of the lens on the collimated optical beam. The nullifying lens is naturally not attached to the phase shifting lens and hence stays fixed in the optical beam.

The focal length of the phase shifting lens can now be calculated. Using the phase shift of 0.1875 mr as an example,

$$\text{Tan } \delta = \frac{\text{disp} \quad r\alpha}{F_L}$$

$$F_L = \frac{r\alpha}{\delta} = \frac{0.00156}{0.0001875} = 8.32''$$

2.5.4 SCANNER INTERLACE GEOMETRY

With a 2.669 inch focal length IR imaging lens, the angle β for a typical system is 0.75 milliradian. See Figure 2-41. The scan/interlace mirror is in front of the lens and hence the interlace motion must tilt the collimated optical bundle 0.75 milliradian in elevation.

Figure 2-42 shows the physical arrangement of a typical system. Rotation about axis 2-43 generates the β angular motion. The motion ϕ about the interlace axis can be resolved into rotations α and β, azimuth and elevation respectively. The relationship is shown in Figure 2-43. Rotating ϕ translates point A to A', hence ϕ can be resolved into α & β, where $\alpha = 0.866\,\phi$ and $\beta = 0.5\,\phi$. Image motion is 2:1 with α and 1:1 with β. Since $\phi = 2\,\beta$ and the required $\beta = 0.75$ mr, the required interlace axis rotation = 1.5 mr.

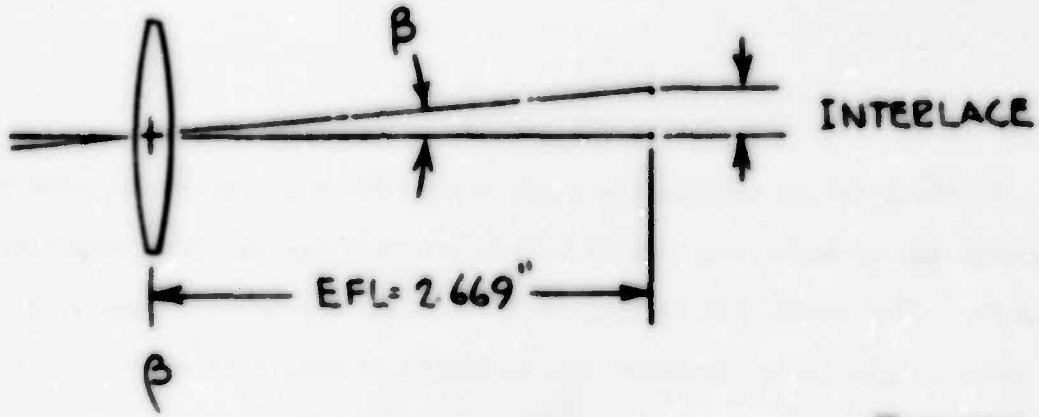


FIGURE 2-41

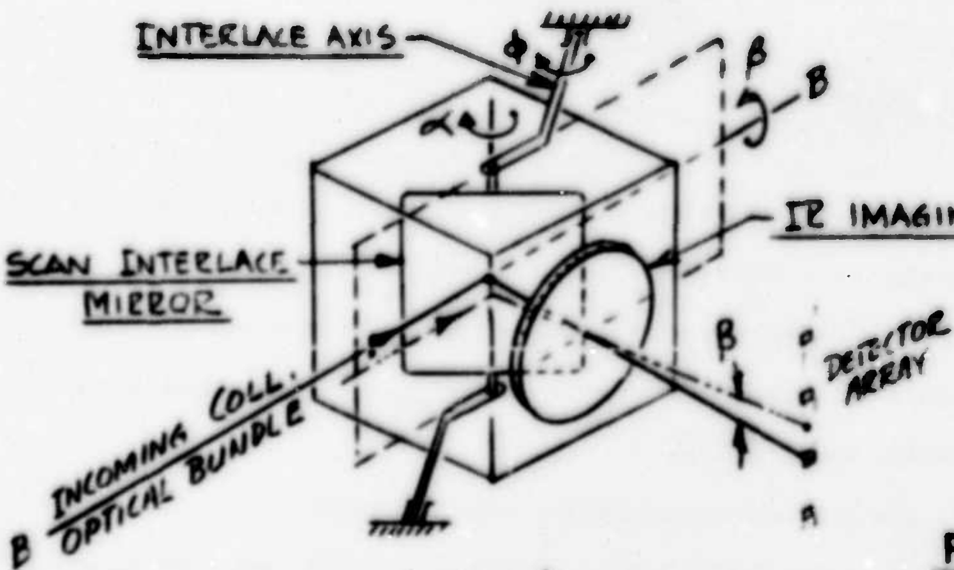


FIGURE 2-42

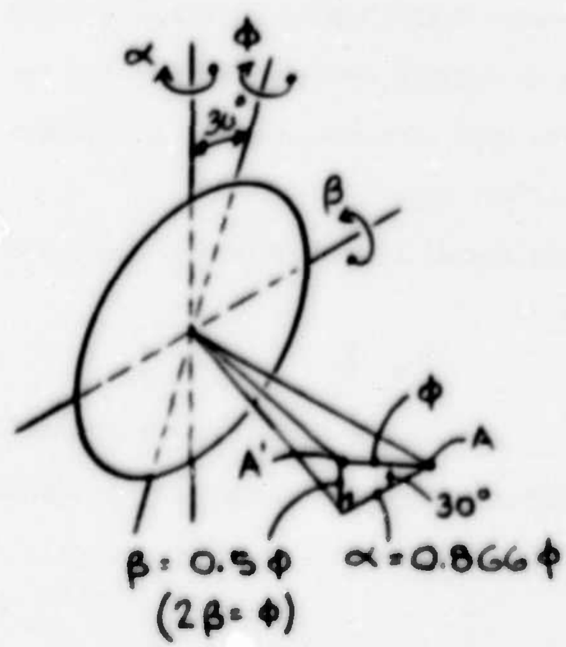
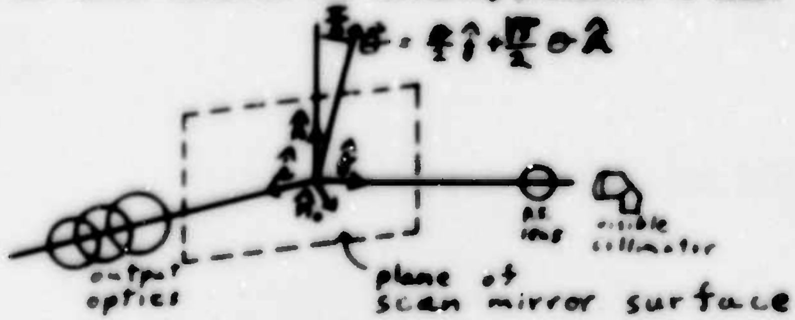


FIGURE 2-43

1/22/75 REB

2.5.5 PHASE SHIFT LENS-VECTOR DERIVATION

In the previous section the phase shift lens calculation was made using standard scalar equations. An alternate approach can be taken using vector notation. The simplicity of this notation makes the analysis easier to follow. In order to use vector notation the following procedure is used.



Set up coordinates about the appropriate axes in the scan module, the x-axis coincident with the nominal output, the y-axis coincident with the input beam from the visual collimator through the phase shift lens, and the mirror scan rotation axis nominally vertical, along the z-axis. Define the following quantities:

$\hat{i}$, $\hat{j}$, $\hat{k}$ are unit vectors along the coordinate axes.

$\hat{n}_o$ is a unit vector normal to the mirror when the scan rotation axis is exactly vertical (whether one interlace coincides exactly or not with this axis depends upon gimbal positio stops and does not affect answer).

$\vec{\theta}$ is the gimbal axis or more precisely, a rotation about the gimbal axis:

$$\vec{\theta} = \frac{\theta}{2}\hat{j} + \frac{\sqrt{3}}{2}\theta\hat{k}$$

Let $\vec{a} = -\hat{j}\,a$ be a vector in the direction of the input. Then $\vec{a}' = a\,\hat{i}$ is the output at center scan when the mirror axis is vertical.

Now allow the gimbal rotation to be applied and find the changes in the mirror normal and output.

$$\Delta\vec{n} = \vec{\theta} \times \hat{n}_o = \left(\frac{\theta}{2}\hat{j} + \frac{\sqrt{3}}{2}\theta\hat{k}\right) \times \left(\frac{\sqrt{2}}{2}\hat{i} + \frac{\sqrt{2}}{2}\hat{k}\right)$$

$$= -\hat{k}\,\theta\frac{\sqrt{2}}{4} + \hat{i}\,\frac{\sqrt{2}\,\theta}{4} + \hat{j}\,\frac{\theta\sqrt{6}}{4} \quad z$$

$$= \frac{\sqrt{2}}{4}\theta\,\hat{i} + \frac{\sqrt{6}}{4}\theta\,\hat{j} - \frac{\sqrt{2}}{4}\theta\,\hat{k}$$

The vector form of the law of reflection from plane mirrors is given in Levi, <u>Applied</u> <u>Optics</u>, Page 347. For a general object a, the image of this object is given by:

$$\vec{a}\,' = \vec{a} - 2\,(\vec{a}\cdot\hat{n})\,\hat{n}$$ where $\hat{n}$ is a unit vector in the direction of the mirror normal.

The initial case of $\vec{a} = -a\,\hat{j}$, $\vec{a}\,' = a\,\hat{i}$ can be checked with this equation.

If we are interested in finding the center scan change in $\vec{a}\,'$ when the gimbal rotates, the plane reflection law may be differentiated.

$$\Delta\vec{a}\,' = -2\,(\vec{a}\cdot\Delta\vec{n})\,\hat{n}_o - 2\,(\vec{a}\cdot\hat{n}_o)\Delta\vec{n}$$

Use the value of $\Delta\vec{n}$ calculated above to determine the output vector change.

$$-2\,\vec{a}\cdot\Delta\vec{n} = +2a\frac{\sqrt{6}}{4}\theta = \frac{\sqrt{6}}{2}a\theta$$

$$-2\,(\vec{a}\cdot\hat{n}_o) = +2a\frac{\sqrt{2}}{2} = \sqrt{2}\,a$$

$$\Delta\vec{a}\,' = \frac{\sqrt{6}}{2}a\theta\left(\frac{\sqrt{2}}{2}\hat{i} + \frac{\sqrt{2}}{2}\hat{j}\right) + \sqrt{2}\,a\left(\frac{\sqrt{2}}{4}\theta\,\hat{i} + \frac{\sqrt{6}}{4}\theta\,\hat{j} - \frac{\sqrt{2}}{4}\theta\,\hat{k}\right)$$

$$= \frac{\sqrt{3}}{2}a\theta\,\hat{i} + \frac{\sqrt{3}}{2}a\theta\,\hat{j} + \frac{1}{2}a\theta\,\hat{i} + \frac{\sqrt{3}}{2}a\theta\,\hat{j} - \frac{1}{2}a\theta\,\hat{k}$$

$$\Delta\vec{a}\,' = \frac{1+\sqrt{3}}{2}a\theta\,\hat{i} + \sqrt{3}\,a\theta\,\hat{j} - \frac{1}{2}a\theta\,\hat{k}$$

The z component of $\Delta\vec{a}\,'$ divided by $|\vec{a}\,'| = a$ is the interlace angle γ.

$$\gamma = \frac{\frac{1}{2}a\theta}{a} = \frac{\theta}{2}$$

The other components of $\vec{\Delta a}'$ can be neglected because they affect the infrared side in a manner which just cancels out the effect on the visible side.

This equation is turned around to give the gimbal rotation angle necessary for the proper interlace angle, γ = 0.75 milliradian.

Now the motion of the phase shift lens may be calculated. Let the position of the phase shift lens be $\vec{r} = r\hat{j}$ as shown in the sketch.

$$\vec{\Delta r} = \text{motion of phase shift lens} = \vec{\theta} \times \vec{r}$$

$$= \left(\frac{\theta}{2}\hat{j} + \frac{\sqrt{3}}{2}\theta\hat{k}\right) \times r\hat{j} = -\frac{\sqrt{3}}{2}\theta r\hat{i}$$

This motion is horizontal as expected. Actually, as r rotates away from ty y axis, $\vec{\Delta r}$ will start to have small components along $\hat{j}$ and $\hat{h}$. However, since only the end points of the motion are used, these components can be neglected.

Thus, the amount of phase shift lens motion is:

$$\Delta x = \frac{\sqrt{3}}{2}\theta r = \frac{\sqrt{3}}{2} 2\gamma r = \sqrt{3}\gamma r$$

Since γ = 0.75 milliradian is the peak to peak interlace angular change, care must be taken to choose the focal length of the phase shift lens so as to produce the peak to peak displacement required. This displacement is usually twice the value calculated in the electronic analysis since it is based on one scan direction only.

2.6 MRT & MDT

The system minimum resolvable temperature (MRT) and minimum detectable temperature (MDT) is a measure of predicting the probability of a viewer recognizing the features in a thermally radiating target.

In order to calculate MRT and MDT, the signal transfer characteristics and noise characteristics of the thermal imaging device and the eyeball must be known. Signal transfer can be represented by the modulation transfer function (MTF) and the noise characteristics are specified by the noise equivalent temperature difference (NEΔT). This section closely follows Ratches development for MRT. We will state the necessary mathematical relationships and not attempted to derive them. The reader is referred to several papers at the end of the text for derivations.

The MTF of a system must take into account the individual MTFs of the various components such as optics, atmosphere, detector, display, eyeball, etc. The transfer functions are the fourier transforms of the geometric spatial functions and the magnitude of the transfer functions is the MTF.

The MTFs of some typical elements are given below:

OPTICS

$$H_{opt} = 2/\pi \left[\cos^{-1} (A) - A \, (1 - A^2)^{1/2} \right]$$

$A = \lambda F_{\#} f_x / l$

λ = wavelength in microns

l = focal length in microns

f_x = spatial frequency (cycles/mr)

DETECTOR

The detector acts as a spatial filter in the horizontal or vertical direction, due to its geometrical angular subtense in the focal plane of the optics.

$$H_{det}(fx) = \sin(\;fx\,X) \Big/ (\;fx\,X)$$

f_x = spatial Frequency
x = Instantaneous F.O.V.

The detector time constant has the effect of limiting the spatial response of the detector as a function of scan velocity

$$H'_{det}(fx) = \left[\frac{1}{1 + (Wx/f_{3dB})}\right]^{1/2}$$

f_{3dB} = 3dB

Point of detector response

ELECTRONICS

The pass band of the electronics also limits the MTF. Using a simple RC circuit roll-off

$$H_{elect}(F) = \left[\frac{1}{1 + (f/fo)^2}\right]^{1/2}$$

fo = frequency
fo = 3-db frequency of roll of network

DISPLAY

If an LED display is used

$$H_{LED}(Fx) = \sin(\pi f x\,X) \Big/ (\pi f x\,X)$$

For a CRT display

$$H_{crt}(fx) = \exp(-a\,f_x^2)$$

assuming a Gaussian spot shape, where a is the variance of the distribution in cycles/mr

MECHANICAL VIBRATION

If vibration can not be removed entirely some blurring will result. Assuming mechanical vibration to be random, another gaussian distribution results.

$$H_{LOS}(fx) = \exp(-P\,x^2)$$

P is calculated from the variance of vibration

EYEBALL

The MTF of the eyeball based on work by Kornfeld & Lawson has the form.

$$H_{eye}(Fx) = e^{-\Gamma fx/M}$$

M = system magnification
Γ = depends on the logarithum of the light level or average display brightness

Table 2-5 Γ as a function of Log Light Level for the Eyeball MTF

Γ	Log (Light Level in fL)
.81333	3
.9598	2
1.0980	1
1.4650	0
1.8300	1
2.2773	2
2.7653	3
3.3347	4
3.9040	5

NEΔT

The noise equivalent temperature difference (NEΔT) of a system is a measure of detector sensitivity. NEΔT based on peak signal-to-rms noise. The equivalent noise bandwidth is

$$\Delta F_n = \int_0^{\infty} S(F)\, H^2_{ELECT}(F)\, H^2_{B}(F)\, H^2_{MD}(F)\, dF$$

S(F) = normalized noise power spectrum

If S(F) is white the equation reduce to

$$\Delta F_n = \pi/2\, \Delta F_e = \pi/2 \left(\frac{1}{2\tau}\right)$$

The inverse of the dwell time τ is given by the number of resolution elements per second, or

$$\frac{1}{\tau} = \frac{\alpha B\, F_R\, \eta_{ovsc}}{\eta\, \Delta X \Delta Y\, \eta_{sc}}$$

α & B are horizontal and vertical fields of view. Fr is the frame rate η_{ovsc} is the overscan rates n is the number of detectors in parallel Δx and Δy are the IFOV's in x and y, and η_{sc} is the scan efficiancy.

For a detector noise limited system

$$NE\Delta T = \frac{4F^2 (\Delta F_n)^{1/2} \sin(\theta/2)}{\pi A \theta^{1/2}\, T_o\, T_a \sqrt{N} \int_{\Delta\lambda} D^{**}_{\lambda}\, N'_{\lambda}\, d\lambda}$$

F is the objective F-number, A_d is the detector area in square centimeters, T_a is atmospheric transmission over the path the NEΔT is measured, τ_o is the optical transmission, $\Delta\lambda$ is the spectral band pass D^*_λ is the shot noise limited specific detectivity which is independent of the detector field of view. N is the number of detectors in series. N_λ' is the temperature derivative of the Planck radiation equation

2.6.1 MRT

The minimum resolvable temperature difference (MRT) in the scanning direction is defined as the minimum temperature difference needed to resolve a standard four-bar pattern with 7:1 aspect ratio oriented vertical to the scan. MRT will be a function of bar frequency. The MRT can be calculated once the NE ΔT and component MTF's have been computed, and its form is derived. In the scanning direction, i.e., the bars oriented vertically, MRT is given by

$$MRT(f_s) = SNR \frac{\pi^2}{4\sqrt{14}} \frac{NE\,\Delta T}{MTF_{TOT}(f_s)} \left[\frac{\Delta y\, v\, f_s\, Q(f_s)}{\Delta f_n\; F_R\; t_E\; \eta_{OVSC}} \right]^{1/2}$$

where

SNR = signal-to-noise ratio necessary to recognize the four-bar pattern.

$MTF_{TOT}(f_s)$ $H_{OPT} \cdot H_{DET} \cdot H'_{DET} \cdot H_{ELECT} \cdot H_B \cdot H_{DISPLAY} \cdot H_{EYE} \cdot H_{LOS} = H_D(f_s)$.

Δy = vertical IFOV in mr.

v = detector scan velocity in mr per second.

f_s = target frequency in cycles per mr.

F_R = frame rate per second

η_{OVSC} = overscan ratio

t_E = eye integration time = .2 second

Q = $\int_0^\infty S(f_s)\, H_N^2(f_s)\, H_W^2(f_s)\, H_{EYE}^2(f_s)\, df_s$

$S(f_s)$ = noise power spectrum out of detector

$H_W(f_s)$ = target filter function of bar-width w.

$H_N(f_s)$ = noise filter function from detector to display.

An MRT in the vertical direction, e.g., bars parallel to the scan direction, can be defined and is given by

$$MRT(f_y) = SNR \frac{\pi^2}{4\sqrt{14}} \frac{NE\Delta T}{MTF_{TOT}(f_y)} \left[\frac{\Delta y \, v \, f_y \, QQ}{\Delta f_n \; F_R \, t_E \, \eta_{OVSC}}\right]^{\frac{1}{2}} .$$

where

$MTF_{TOT}(f_y) = H_{OPT} \cdot H_{DET} \cdot H_{DISPLAY} \cdot H_{EYE} \cdot H_{LOS} = H_D(f_y)$

f_y = target frequency in cycles per mr.

$$QQ = \frac{7}{2f_y} \int_{-\infty}^{\infty} \int_{0}^{\infty} S(f_x) H_N^2(f_x) H_L^2(f_x) H_{EYE}^2(f_x) H_D^2(f_x) H_W^2(f_y) H_N^2(f_y) H_{EYE}^2 \, d^2 f$$

H_L^2 = target filter function of bar length $L = 7W$.

This vertical MRT, in which sampling effects are averaged out, is an attempt to consider the effects of vertical resolution on overall system performance. It is still a controversial quantity and totally unvalidated. However, NVL is actively engaged in pursuing this concept as a measure of system behavior.

Figure 2-46 illustrates the form of MRT. At each frequency f_c, there is a minimum temperature difference ΔT_c necessary to resolve the four bars. There is a frequency f_R at which the MRT becomes infinite (the MTF equals zero), and no amount of signal will resolve the bars. For a system with no degradation after the detector, f_R equals the reciprocal of the IFOV. Although bars can theoretically be resolved beyond this frequency because of the wings of the sinc function, practically it is a limit to system resolution. Real systems attain only 60 to 90 percent of this theoretical cutoff f_R.

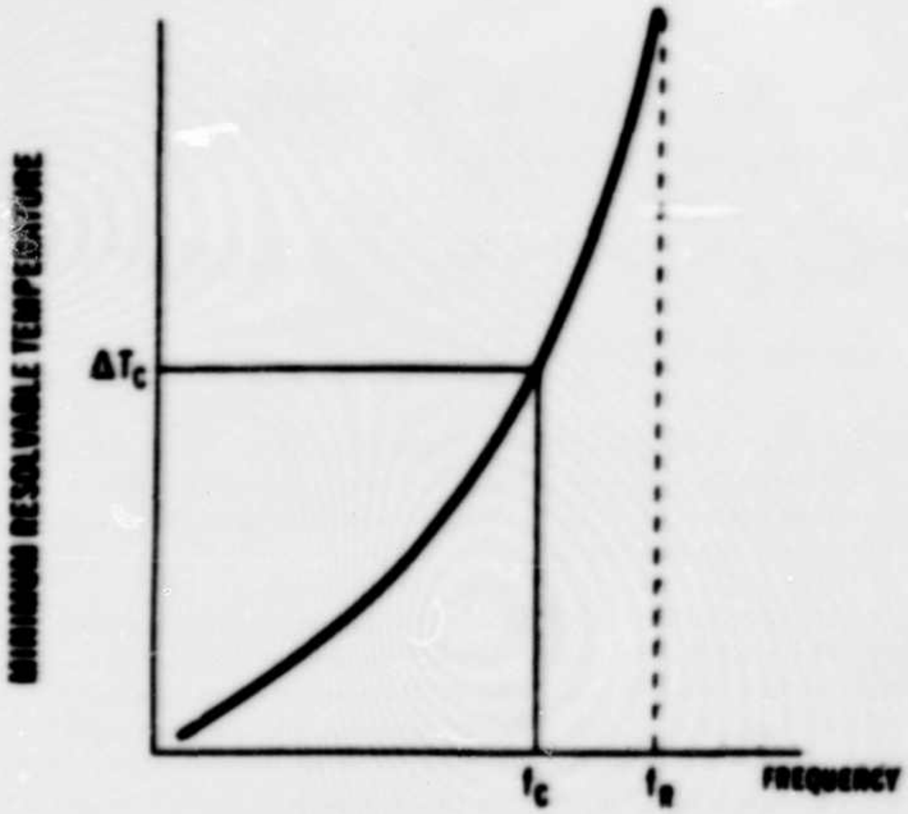


Figure 2-44. Representative MRT Curve.

2.6.2 MDT

The minimum detectable temperature (MDT) of a thermal device is defined as the minimum temperature difference between a square (or circular) target and the background necessary for an observer to perceive the source through the device. MDT is then a function of target size and represents the threshold detection capability of the system. It can be derived from the same signal-to-noise expression as that used to derive MRT. The result is

$$MDT = \frac{NE\Delta T \, S'}{A_T \int_{-\infty}^{\infty} H_T^2 \, H_D^2 \, d^2 f} \left[\frac{\Delta y \, v}{\eta_{ovsc} \, F_R \, t_E \, \Delta f_R} \right]^{1/2}$$

$$\cdot \left[\int\!\!\int_{-\infty}^{\infty} S(f_x) \, H^2_{ELECT} \, H^2_{DISPLAY} \, H^2_{EYE} \, H_T^2 \, H_D^2 \, d^2 f \right]^{1/2}$$

where

A_T = target area in square milliradians

S' = threshold signal-to-noise ratio

H_T = target transform = $H_L \times H_W$

H_D = total device and eyeball MTF = MTF_{TOT}.

Figure 2-45 illustrates the form of MDT as a function of reciprocal target size. For any target size α in milliradians, there is a ΔT_D which is the minimum temperature difference necessary for the target to be detected. There is no asymptote for MDT as there is for MRT since any size source can be detected if hot enough. An arbitrarily small target can be detected if its signal strength is large enough to excite one IFOV, i.e., a thermal device is capable of "star detection."

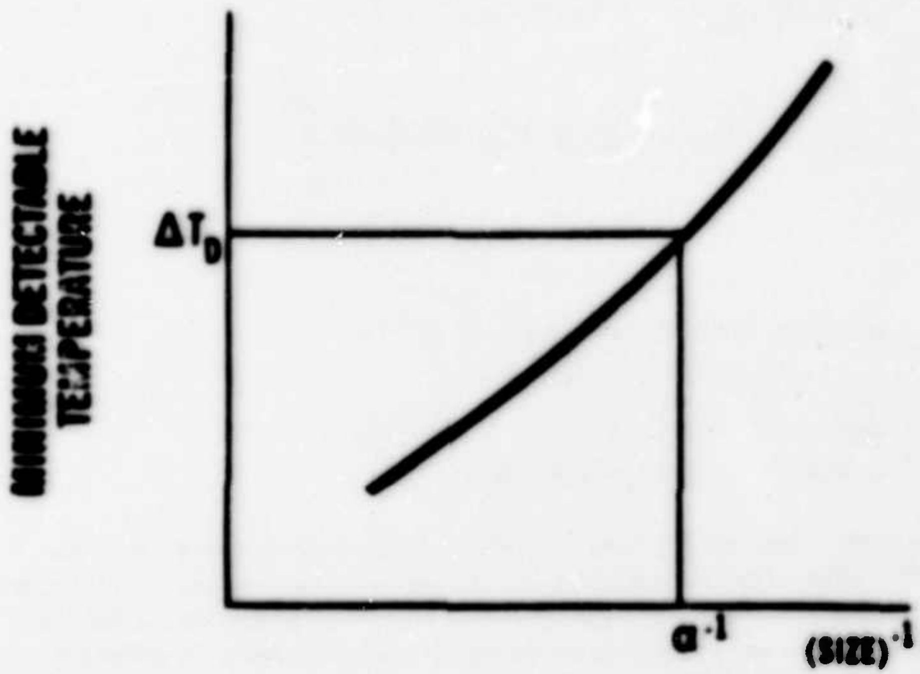


Figure 2-45. Representative MDT Curve

References:

Night Vision Laboratory Static Performance Module for Thermal Viewing Systems James A. Ratches et al NTIS-AD-A011 212

SECTION III

SYSTEM DESIGN CONSIDERATIONS

3.1 THERMAL DESIGN CONSIDERATIONS

Although the individual module power dissipations are, with the exception of the Cooler-Inverter, very low, adequate thermal system design is essential for satisfactory performance of the system.

The estimated dissipation of each module is as follows:

Bias Regulator	.03 Watt/Channel (180 channels max)
Detector-Dewar/Bias Pack	.013 Watt/Channel (180 channels max)
Preamplifier	.61 Watt/module (20 channels)
Postamplifier	1.67 Watts/module (20 channels)
Auxiliary Control	2.24 Watts
Scan-Interlace	3.00 Watts (60 Hz unit)
Scanner	2.00 Watts
LED Array	1.50 Watts
Cooler-Inverter	55.00 Watts (44 in cooler, 11 in inverter)

The power dissipated by the first four modules listed is a function of the number of channels used in the system. In the cases of the Preamplifier and Postamplifier, more than one of each module may be required, up to a maximum of nine of each. The cooler poses the greatest problem for system thermal design both because it has the highest thermal dissipation and because its detector cooling performance deteriorates at elevated temperatures where good performance is most needed to carry the increased thermal load on the cold finger. It is most important to minimize the helium temperature in the cylinder. The cylinder is heated by the compression temperature rise of the helium gas, by mechanical friction, and by conduction of heat from the motor. The heat dissipated in the Cooler is about equally divided between the electrical losses in the motor and the mechanical work in the compressor. Natural convection even combined with conduction to conventional mounting structure is not adequate to prevent excessive cylinder temperature rise. Either foced convection with added finned surface on the cylinder head, or a heat exchanger attached to the cylinder head, or a combination of convection and heat exchanger must be used. If the system is to be designed with a sealed case,

excluding ambient air from direct contact with the modules, it may be desirable to provide a heat exchanger sealed from the internal air in the case, through which ambient air is blown by a fan. The heat exchanger can be used as the mounting structure for the modules. In particular, the cooler would be mounted with its cylinder head attached directly to the heat exchanger for good thermal contact. The Cooler should be located near the coolest part of the heat exchanger, that is, near the cooling air inlet before the air is heated by other modules in contact with the heat exchanger. The inverter is completely enclosed in a nickel-iron sheet metal case. The major heat dissipating components are mounted on the inverter base plate or on brackets attached to the base plate. Therefore, the inverter is best cooled by mounting its base directly on a heat sink such as the heat exchanger described previously.

Although the power dissipation of the other five individual electronic modules is low, the cumulative dissipation can amount to a very significant amount, especially if the system uses a large number of detector channels. Typically this can amount to almost 20 watts for a 100 channel system. The thermal problem in these modules is increased if, as is usually done, a complete sheet metal shield encloses this group of modules for EMI protection. The use of a printed wiring mother board for interconnecting these modules further adds to the thermal problem by forming a thermal barrier on the bottom. Several alternatives may be considered to overcome the thermal problem . The relative need for any degree of shielding which must be designed into a particular system may permit elimination of all or part of the sheet metal shield or the substitution of a screen shield. This would improve convective cooling of these modules. Sheet aluminum partitions with a finish for high thermal emissivity may be located between modules to receive heat from the modules by radiation and convection. They then conduct the heat out to where it can be removed by conduction to the heat exchanger or by convection to ambient air.

Another possible alternative involves the use of a small fan in the main system housing, which blows air through shielded openings in the sheet metal shield to cool the inside modules by forced convection. Although these modules can operate in any attitude, heat transfer by natural convection from the components to the shield or to the partitions previously mentioned is best if the module circuit boards are mounted vertically. If forced convection is used, the mounting attitude is unimportant.

The Scanner, Detector-Dewar/Bias Pack, and LED Array dissipate little power relative to their sizes. They therefore can often rely on conduction through their mounting surfaces, plus natural convection, to transfer heat to the system housing. However, in the over-all system thermal design it may be desirable to provide conductive paths from these modules to a heat exchanger to reduce the general internal temperature in the system housing.

The thermal design of any system must of course include consideration of the heat dissipated by not only the common modules, but also any system unique modules such as power supplies, fans, and displays. In general, the outside surface of the system housing is not normally sufficient to provide adequate system cooling by natural convection and radiation without seriously degrading performance or reliability or both as a result of excessive internal component temperatures.

The optical modules in any system of course do not contribute to heat dissipation other than the small and intermittent amount which may be given out by an electrical focus control. However the optical modules must be considered in the system thermal design. Temperature of the optical elements affects the index of refraction of each lens element. The expansion coefficients of the elements and the lens mounts produce dimensional changes.

These effects can cause significant changes in focal length. In addition, thermal expansion of the structure supporting the various parts of the optical system can result in degraded focus and misalignment of the optical images. The IR Imager module does have focus adjustment which may be used to refocus the IR image. No visual focus adjustment, other than initial shimming, is provided in the common modules. Thermal factors must be carefully considered in selecting the materials and laying out the design of the system structure and the mounting brackets supporting the optical modules so as to minimize temperature effects on focus and alignment.

3.2 <u>RELIABILITY AND MAINTAINABILITY CONSIDERATIONS</u>

The inherent reliability and maintainability of the common modules, a function of their design, including choice of components, derating of components, etc., cannot be improved at the time of their installation and operation in a system. What must be done, however, is to ensure the inherent reliability and maintainability of the modules are not degraded by the manufacturing process or by their application in a system. Modules must not be used outside the range of their specifications, and the system design must consider the following design requirements:

(a) Thermal requirements

(1) adequate ventilation

(2) sufficient heatsinking

(3) forced air cooling if necessary

(4) module location for maximum heat dissipation

(b) Mechanical requirements

(1) mounting compatible with size and weight of module and shock and vibration requirements.

(2) captive type hardware wherever possible.

(3) easily accessible adjustment controls and test points.

(4) capability of removing a specific module without removal of other modules.

3.3 SYSTEM OPTICAL DESIGN CONSIDERATIONS

3.3.1 RESTRICTIONS ON OPTICAL MODULE OR RECTICLE CONFIGURATION

The optical modules IR imager, visual collimator, and scanner may be assembled into systems in a variety of ways, one of which is shown in Figure 3-1. It may be appropriate here to point out some of the restrictions on the configuration of systems.

(a) The scan mirror has one-side coated to maximize reflectance of 6600 Å LED light and the other side is coated to optimize 7.5 -11.75 micrometer reflectance. Therefore the IR components may interface with only two sides of the scan module and the visual system with the other two sides.

(b) The modules must be used so as to provide an erect image in the display with the proper reversion-left on left, etc.

(c) The modules must be assembled so that the operation of the interlace affects both IR and visible sides consistently. It is possible to have the proper inversion & reversion of the display relative to IR object space, and still have oneside interlace up when the other side is interlacing down.

(d) In some systems there is a requirement that the operator viewing the display be facing in the same direction that the IR or "taking" optics are looking.

(e) Narcissus effect - The detector dewar presents an extremely cold target which the detector itself may see if there are reflections from the optical surfaces. There is one or two percent reflectance left in the best AR coating. This radiance from extremely cold target is a significant signal, particularly if it is in focus.

There are several techniques to counteract the narcissus effect. One is to use the best AR coatings available. Another is to monitor the IR afocal design to insure that all possible reflections of the focal plane do not return in focus to the focal plane the farther they are out of focus the better.

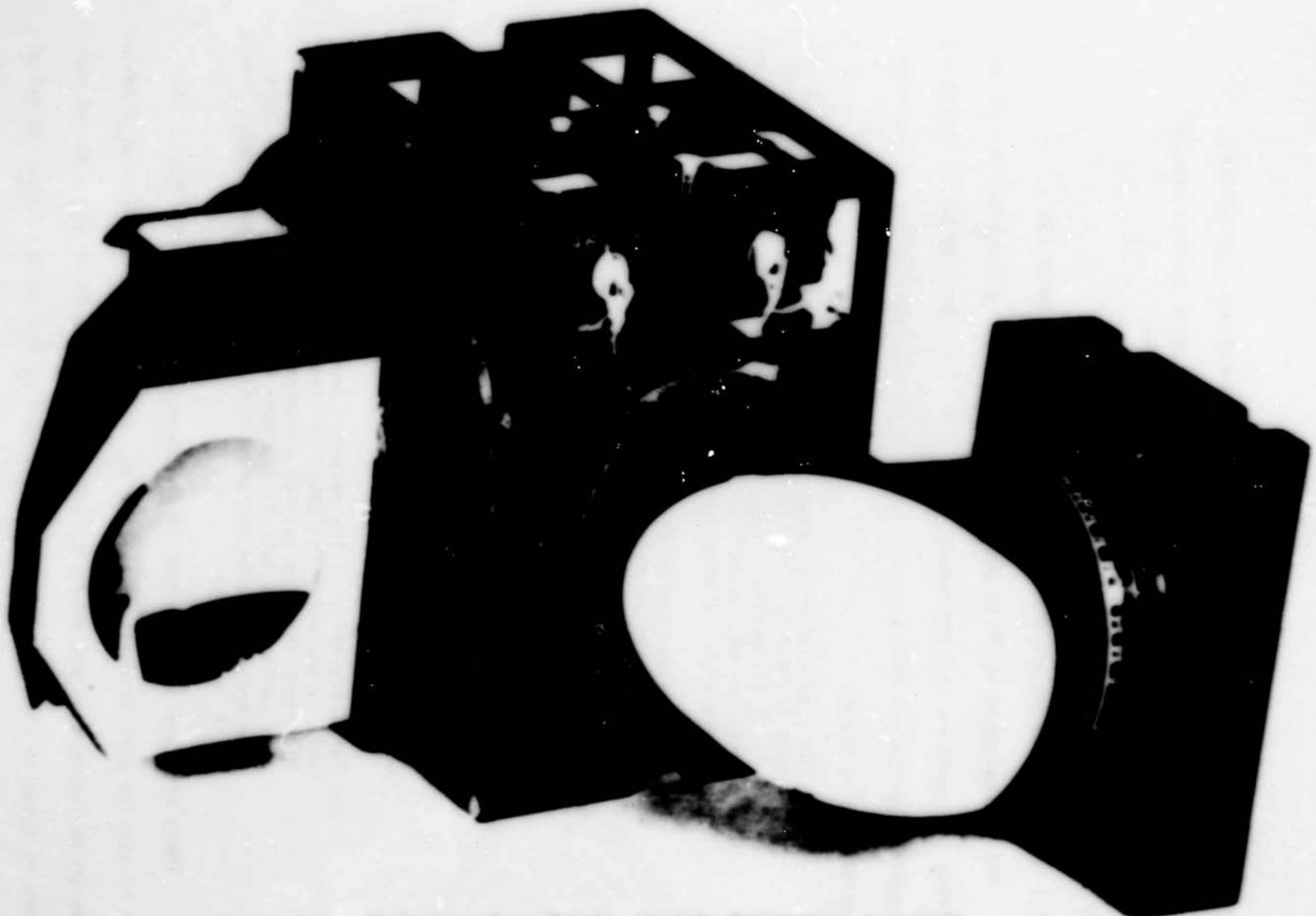


Figure 3-1. IR Imager, Scan Module, Visible Collimator, and Light-Emitting Diode Module.

Only afocal lens elements need to be bent so as to avoid narcissus because they are ahead of the scan mirror. The IR imager lens elements will not cause time varying reflections in the detector and the detector produces no signal from them.

The module system design provides space between the IR imager back flange and the detector dewar for the placement of an external cold shield; which is a third fix for narcissus. The primary purpose of this shield is to block background radiation from portions of the solid angle which are not used in the particular system. This raises the effective D* of the detector plane back on itself. A secondary effect of an external cold shield is to reduce the cold dewar object size, which minimizes the narcissus. Finally, any IR windows ahead of the objective must be tilted or converted into domes with weak optical power. This must be done because a flat plate in a parallel beam autocollimates the IR optical system perfectly.

(f) Vignetting between afocal & IR Imager must be avoided in a FLIR design.

This problem is a generic one for Galilean afocal lenses coupled to the IR imager through the scanner. The aperture stop should be placed as far forward as possible in order to limit the diameter necessary on the large front elements of the afocal. But the farther forward it is placed, the farther forward is the exit pupil of the afocal. The amount of apparent side-to-side motion of the exit pupil as seen at the IR imager increases with the optical lever arm-the distance between the afocal exit pupil and the scan mirror pivot. A condition can occur in which the bundle of incoming radiation actually moves with scanning so far laterally that it goes off the clear aperture of the first IR imager element. In this case there is a change in

in the amount of radiation from the target scene relative to radiation from the (probably hotter) inside parts of the system. This can be seen by the detector as a spurious signal. Thus one of the basic tradeoffs in the design of afocal lenses for the common module systems is the position of the stop.

(g) Athermalization

The infrared optics has a significant change in some of its parameters when operating over large temperature ranges. Not only do the focal lengths tend to be longer in the infrared afocal, but the dN/dt's of the optical matrials are from ten to one-hundred times larger. In order to minimize the number of possible sources of defocus, it is desireable to have as many lens assemblies-modules as well as system unique components-automatically compensate for temperature changes.

This had not been accomplished in the IR imager by the selection of materials or complicated lens mounts on stacks of rods. The athermalization is accomplished by screwing the front doublet in or out by means of a gear. This would allow the addition of a temperature controlled servo to adjust the focus. The IR imagers from different manufacturers are alike with respect to function, but not to the optical power. If a module of one type is substituted for another the amount of temperature controlled adjust required is likely to be slightly different.

CHAPTER 2

PREAMPLIFIER, VIDEO, INFRARED

USAECOM SM-D-773663

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Infrared Video Preamplifier module hereinafter called the preamplifier provides amplification and processing of the video signal outputs from a detector array of an infrared system. Each preamplifier module (printed wiring board) contains four integrated circuits (IC) chips each providing 5 channels for a total of 20 channels per module.

1.2 INTENDED USE OF ITEM

The Preamplifier module has been designed to be interfaced with other major common and special modules to form an integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The function of the preamplifier in the system is to amplify and process the outputs of the individual elements of a detector array to a useable level. With each preamplifier providing 20 channels, the number of modules required per system will depend upon the number of channels required by the system being designed.

1.3 TECHNICAL SPECIFICATIONS

The technical specifications of the Preamplifier module are as follows:

Parameter	Specification
Gain	70 ± 7 volts/volt
Band width	
Upper 3dB Frequency	105±25kHz
Lower 3dB Frequency	4±2Hz
Flat (±0.5db of midband gain)	30Hz to 30kHz
(midband gain reference: 0dB at 1kHz)	

Parameter	Specification
Equivalent Input Noise	1.5×10^{-9} Vrms/$\sqrt{Hz}$ (max)
Equivalent Input 1/f Noise	$<10 \times 10^{-9}$ vot/$\sqrt{Hz}$ at 100Hz
Channel Crosstalk (1mVrms at 1kHz input)	≤ -30 dB
Maximum Input (Output distortion 5%)	0.01 Vpp at 1 kHz
Recovery Time with Input of 50 msec, 0.01 volt pulse representing a projectile signal of 0.7 mV, 10 msec wide	<0.2 seconds
Input Impedance	4000 to 6500 ohms (5000 ohms nominal)
Output Impedance	400 to 700 ohms (500 ohms nominal)
Supply Voltage and Currents	
High Power (Input P1-7&8)	8.5 to 10 volts dc, 55±6 mA
Low Power (Input P1-2,3, P1-7&8 open)	3 ±0.3 volts dc, 44 ±5 mA

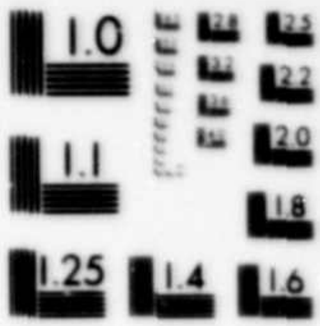
NOTE

For interface information such as mechanical configuration, outline dimensions, electrical interconnection and mounting information, refer to Section III.

AD-A118 049 MAGNAVOX GOVERNMENT AND INDUSTRIAL ELECTRONICS CO MA--ETC F/G 9/5
PRELIMINARY COMMON MODULE DESIGN HANDBOOK.(U)
APR 76 DAAG53-75-C-0178
UNCLASSIFIED GSDR-900 NL

2 OF 5
AD
A118049

18049



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

As shown in Figure 2-1, Preamplifier Module Schematic Diagram, the preamplifier module contains 4 integrated circuit (IC) amplifier chips with five amplifier channels per chip, thus providing 20 signal processing channels per module. The chip itself is packaged into a dual inline (DIP) package. The module also provides a voltage regulator in addition to the four IC amplifiers and their peripheral components. The regulator converts a nominal 9.5 volt input to a 3.6 volt Vcc for amplifiers. Alternately, the Vcc for the amplifiers may be supplied from the system power supply by connecting the appropriate voltage to pin 23 of the module connector P1.

The preamplifier modules have no potentiometers or other controls, are gain stable, and are directly interchangeable without adjustment.

2.2 THEORY OF OPERATION

2.2.1 IC AMPLIFIER

Each of the five amplifier channels within the IC consists of six NPN transistors as shown in the schematic Figure 2-2. The first transistor is basically diode connected and serves to set the bias of a three transistor operational amplifier. The channel gain of 70±10% is established by a resistive feedback network around the operational amplifier. The two output transistors are followers with feedback from the first output transistors to the input bias setting transistor. This is done to improve linearity and recovery with high input signals. The final output transistor has a resistor divider in the emitter, with the output taken from the center tap of the divider to improve stability with capacitive loads and to provide uniform output impedance.

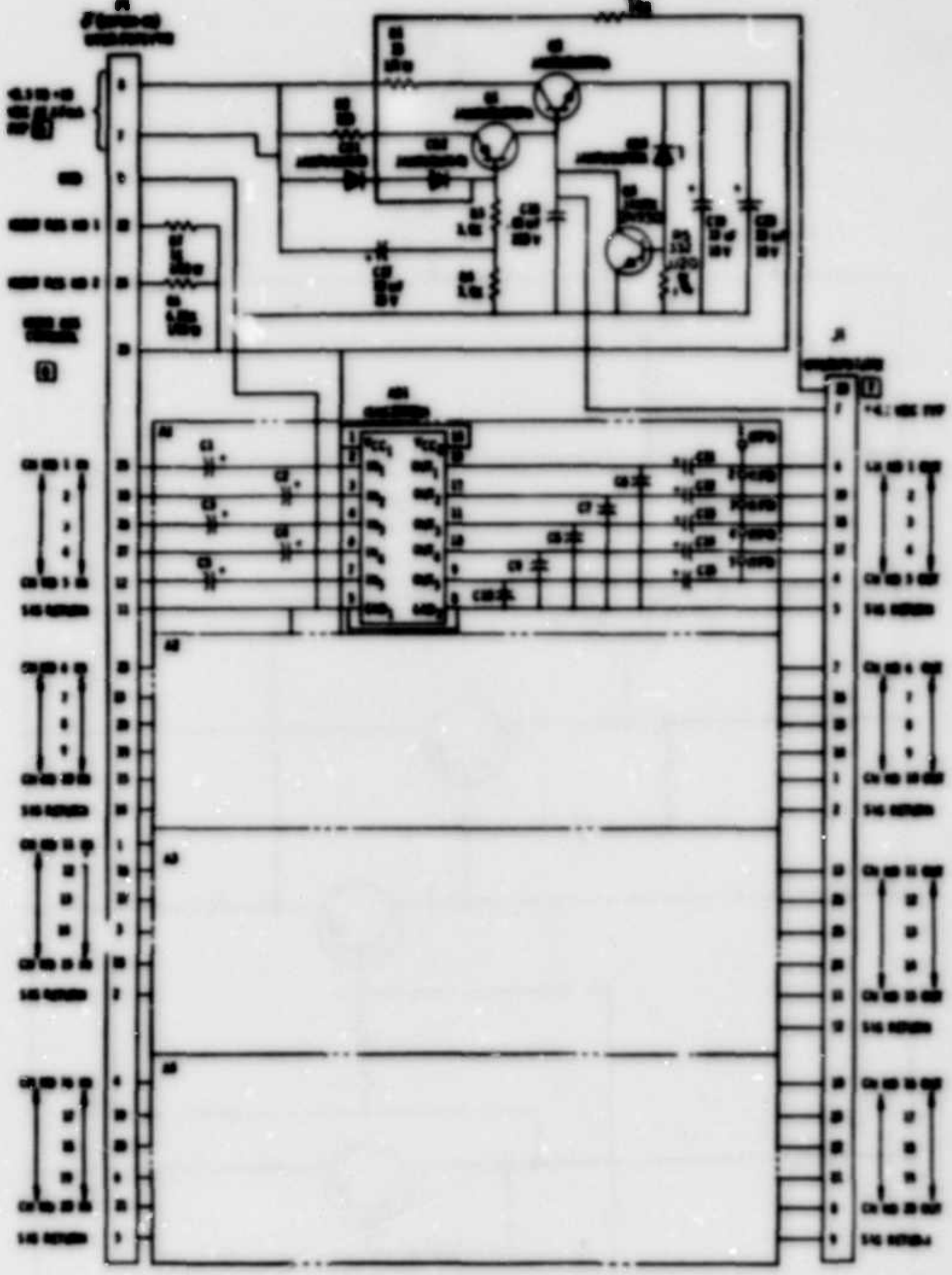


Figure 2-1. Preamplifier Module Schematic Diagram

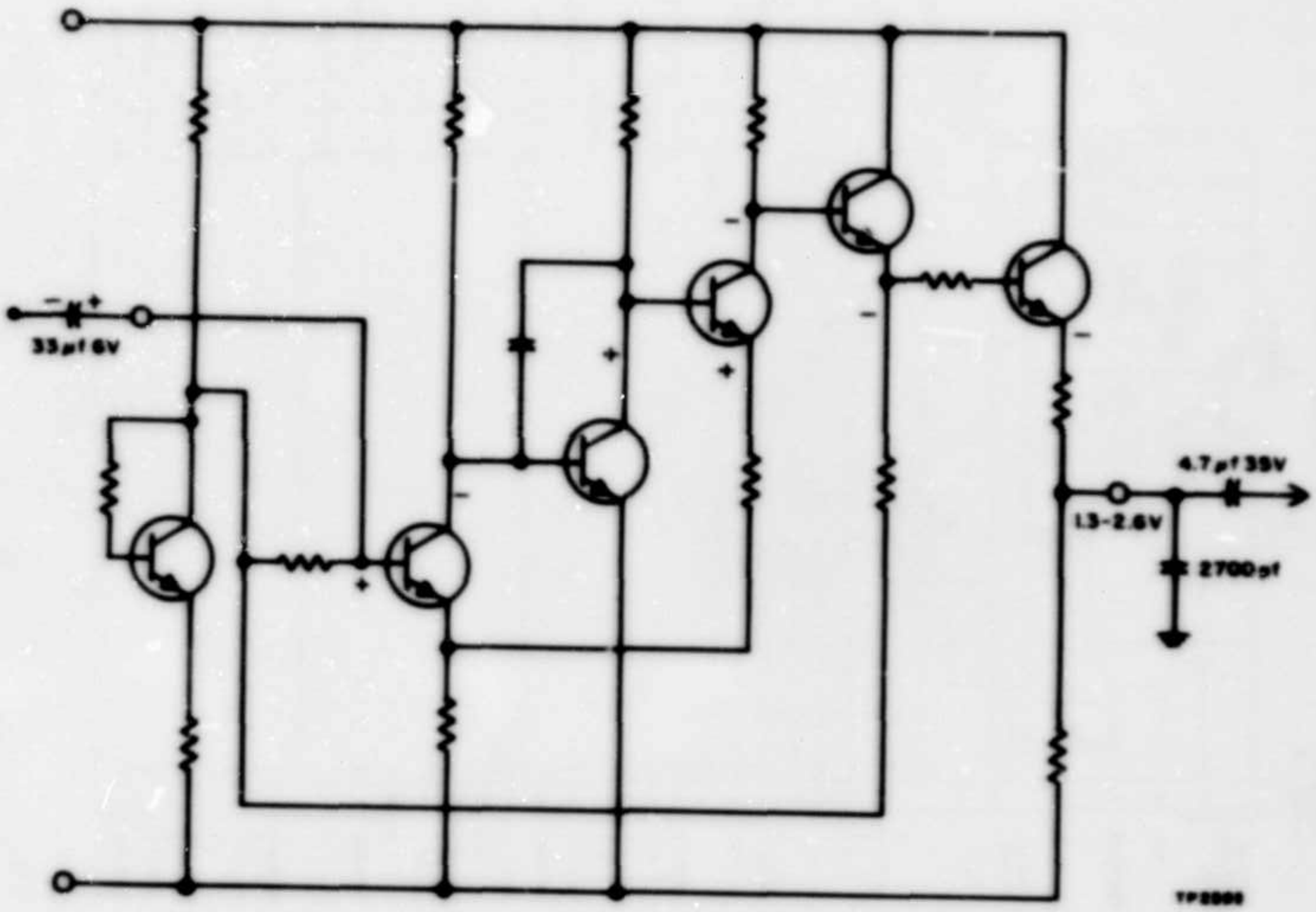


Figure 2-2 Preamplifier IC Schematic Diagram

2.2.2 AMPLIFIER CHANNEL OPERATION

Since operation of the twenty video channels is identical, only operation of one channel will be covered in this description.

Channel 1 video signal from the channel 1 detector element enters the module through connector pin P1-25 and is AC coupled to the input of amplifier A1AR1 by a 33 uf, 6V capacitor (C1). This capacitor in conjunction with the input impedence of the amplifier (5K ohms) gives a low frequency break point of approximately 1Hz. The 500 ohm output impedence of the amplifier and 2700 pf capacitor C6 establish the high frequency rolloff at 118KHz. The dominant low frequency characteristic of the preamplifier is established by a 4.7 uf output coupling capacitor (C11) and the input impedance of the post amplifier module which is 10K ohms. This combination gives a low frequency 3db point of 3.4Hz.

2.2.3 VOLTAGE REGULATOR

The IC amplifiers described above have a power supply rejection ratio (PSSR) of approximately 30dB referred to the input. In order to increase the PSRR and thereby reduce the power supply ripple as seen at the preamplifier input to a factor of 3 below the wideband equivalent input noise, a voltage regulator is provided on each preamplifier module which operates as follows:

The 7.5 to 10 volt dc input power is supplied to the regulator through module input connector pin P1-8 (Figure 2-1). Diodes CR1, CR2 and resistors R3 and R4 form a voltage divider to establish the base bias for transistor Q1. Transistor Q1 acts as a constant current source which supplies the base drive for series pass transistor Q2. The emitter of Q2 supplies the regulated 3.6 volts dc to the IC amplifier chips.

Zener diode CR5 and resistor R5 form an output voltage sensing network. If the output voltage increases, the sensing network increases the base drive to transistor Q3 which in turn reduces the base drive applied to series pass transistor Q2. If the output voltage tries to decrease, the regulating action is reversed and the base drive to Q3 is increased to increase the output voltage. Thus the output voltage is maintained at 3.6 ±0.3 volts dc.

SECTION III

INTERFACE

3.1 CONFIGURATION

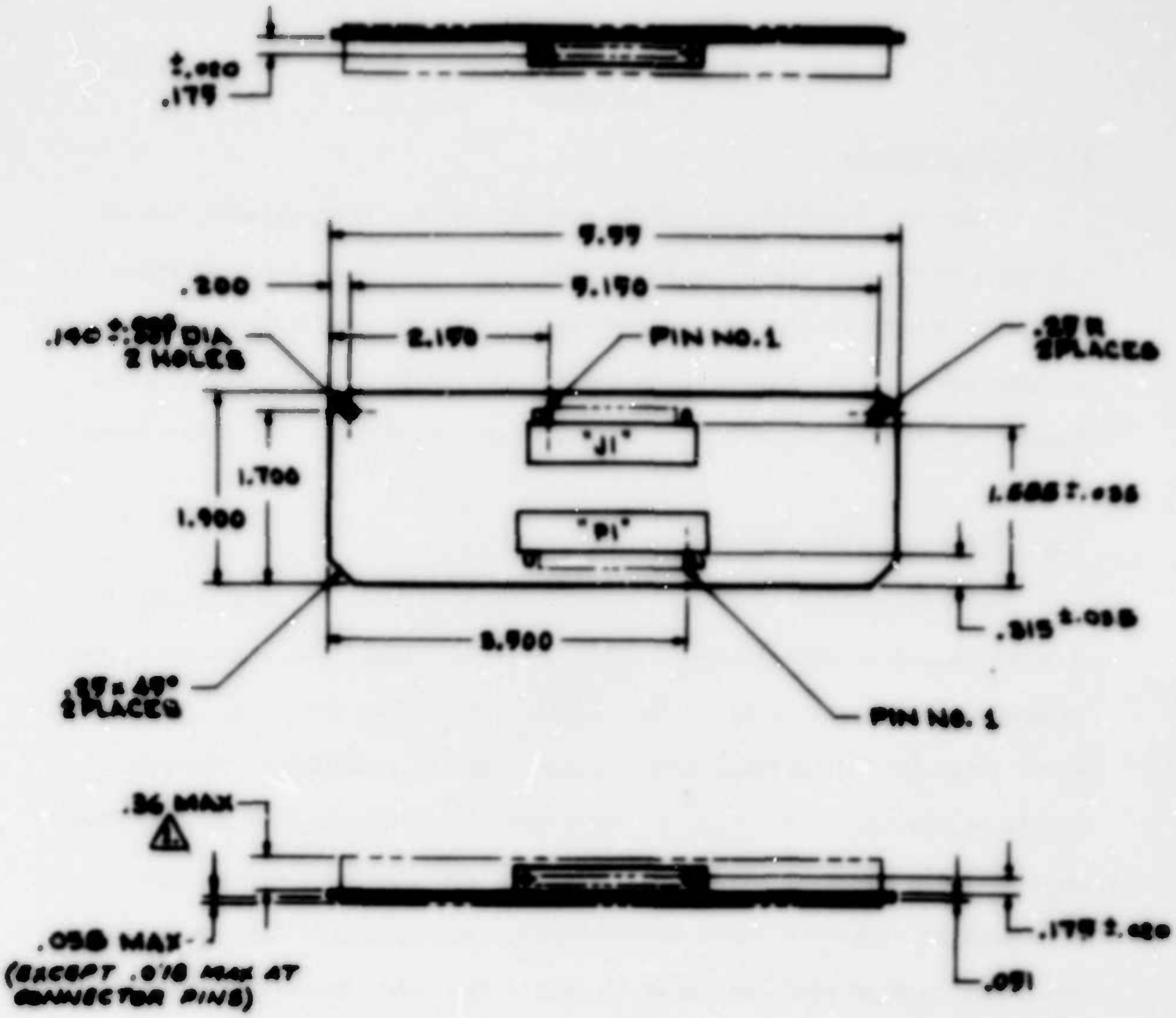
Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating the Preamplifier module in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is a photograph of the module and Figure 3-3 is a parts location drawing.

3.2 INTERCONNECTING INFORMATION

The input signals and power are connected through P1 to a connector on a mother board or wiring harness through which connections are made to the Detector and a power supply. The output jack J1 ties to a cable connector which leads to the Postamplifier. Access must be provided to the test points at the top of the module. Each end of the module must be supported by a suitable mounting slide. For applications involving severe shock or vibration, positive means should be provided to retain the module in the fully engaged position, also to retain the cable connector which engages with J1.

3.3 THERMAL DESIGN CONSIDERATIONS

Although the indididual Preamplifier module power dissipation is only 0.61 watts per module, very small in an overall system, it must be taken into account during system design. Refer to Section III Chapter 1 for a discussion of the system thermal design considerations.



Tolerances:
.xx = ±.02
.xxx = ±.010

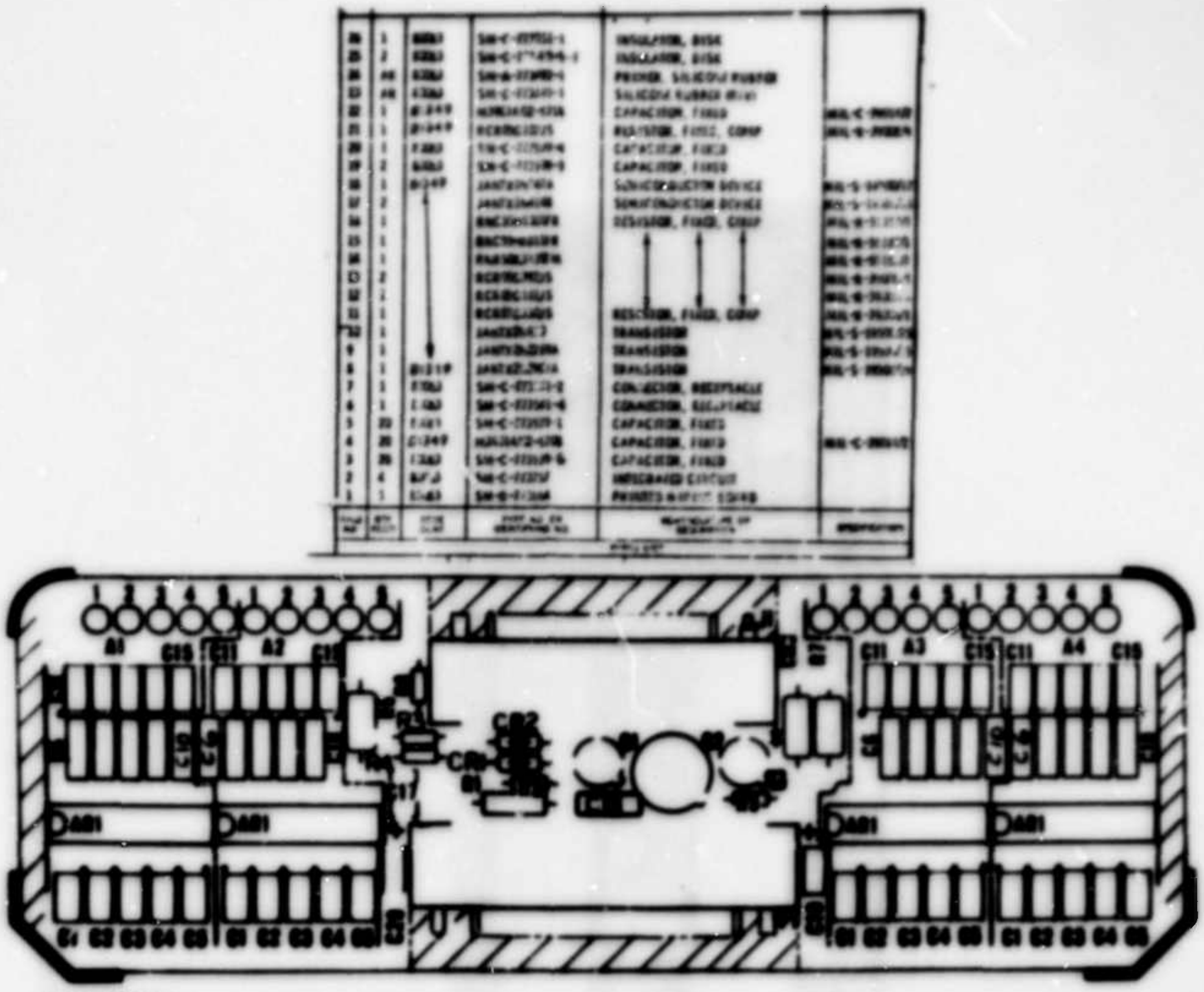
NOTES:

⚠ B2-28A080106 SPEC DENOTES THIS DIMENSION AS .34 MAX.

TP8007

Figure 3-1 Preamplifier Module Outline Drawing

Figure 3-2 Photo of Preamplifier Module



SM-D-773663

TP2844

NOTE: Reference designations for each nonremovable identical stage are assigned by prefixing with A1-A4

Example: C1 is A56A1C1 on Stage A1
C1 is A56A2C1 on Stage A2
C1 is A56A3C1 on Stage A3
C1 is A56A4C1 on Stage A4

Figure 3-3. Preamplifier Module Parts Location Drawing

3.4 ELECTRICAL INTERFACE DATA

3.4.1 INPUT CHARACTERISTICS

(a) Impedance: 4000 to 6500 ohms

(b) Signal: sinewave with 0.01 volt peak-to-peak, maximum, at 1 kilohertz

(c) Voltage: 3.0 ±0.3 volts dc or 8.5 to 10.0 volts dc

(d) Current: 44 ±5 milliamperes at 3.0 volts dc or 55 ±6 milliamperes at 8.5 to 10.0 volts dc

(e) Equivalent input noise voltage: 1.5×10^{-9} volts rms/$\sqrt{Hz}$ maximum

(f) Equivalent input 1/f noise: $< 10 \times 10^{-9}$ volts/$\sqrt{Hz}$ measured at 100 Hz

3.4.2 OUTPUT CHARACTERISTICS

(a) Impedance: 400 to 700 ohms

(b) Voltage gain: 70 ± 7 volts/volt

3.4.3 PROCESSING CHARACTERISTICS

(a) Signal bandwidth: with a 10 kilohms load, upper 3dB frequency 105 ±25 kHz; lower 3dB frequency 4 ±2 Hz; gain-flat (±0.5dB of midband gain) from 30 Hz to 30 kHz (midband gain reference: 0dB at 1 kHz)

(b) Recovery time: $<$0.2 second from a 50 millisecond, 0.01 volt pulse input representing a blast to display a projectile signal of 0.7 millivolt amplitude and 10 millisecond width

NOTE:

Recovery time is measured from trailing edge of pulse input to leading edge of projectile signal)

(c) Channel crosstalk (19 channels into 1 channel): < -30 dB with a peak input voltage (e_{in}) of 1.4 millivolts (1 millivolt rms) at 1 kilohertz, when

$$\text{Channel crosstalk} = 20 \log \left[\frac{19 e_{out20}}{e_{out1} + e_{out2} + \ldots e_{out19}} \right]$$

(d) Noise figure (F_n): F_n 5.7 dB where

$$F_n = 20 \log \left[\frac{\text{total rms voltage at the output}}{\text{total rms noise voltage at output due to source resistance } R_s \text{ alone}}\right] R_L = 10 \text{ kilohms}$$

(e) Channel-to-channel tracking: maximum variation in normalized voltage gain of each channel is ±5% of average gain on 20 channel preamplifier over temperature range of -54 to +71°C

(f) Voltage gain drift: maximum variation in average voltage gain of 20 channels on each preamplifier is ±10% of average gain at ambient, over operating temperature range of -54° to +71°C

3.4.4 ANCILLARY ELECTRICAL DESIGN CONSIDERATIONS

(1) If a regulated 3.0 ±0.3 volt dc is being supplied from the system unique power supply to power the preamplifier (connector P1, pin 23, on schematic diagram Figure 2-1) in lieu of an unregulated 8.5 to 10 volts dc (connector P1, pins 7, 8), the 3.0 ±0.3 volts dc should not have a ripple and noise content that exceeds 15 microvolts.

(2) Input and output channel signal leads to and from the preamplifier should not be routed adjacent to each other. In addition, to avoid extraneous pickup, the input channel signal leads should be kept away from other high amplitude and or high frequency signal sources.

(3) Do not locate the preamplifier assembly adjacent to or near strong electromagnetic or electrostatic fields. If so located, appropriate sheilding of the preamplifier might be required.

(4) The "Voltage Gain" and "Signal Bandwidth" values specified in 3.4.2 and 3.4.3 are valid only if the preamplifier load is 10,000 ohms. For other load values, the voltage gain and signal bandwidth will change accordingly.

3.5 DESIGN LIMITATIONS-GENERAL COMMENTS

The preamplifier module is intended to be used with photoconductive Hg:Cd:Te detectors. These detectors are characterized by low impedance, on the order of 50 ohms and low noise. Use of the preamplifier module with photo-voltaic or high impedance photo-conductive detectors is generally not recommended. Optimum utilization of photovoltaic detectors require a current mode preamplifier which maintains the detector at or near a zero bias condition. Use of the preamplifier with photoconductive detectors of an impedance level many times greater than the 5K input impedance of the preamplifier results in signal loss at the detector/preamp interface. By interposing a simple follower connected FET stage between the detector and the preamplifier the preamplifier could be effectively used, however. It is to be noted that this crosstalk minimizing and localizing technique is continued through the signal processing with an individual signal return associated with each five channel IC chip. Because of the low noise requirements, the preamplifiers use a single ended rather than differential input design. While the single ended design gives a noise improvement of $\sqrt{2}$ over the differential design, there is no common mode rejection. The on-board regulator aids in minimizing power supply noise and ripple when the module is used in the "High power" mode. In this mode, the regulator provides ripple rejection of approximately 67dB. For low power applications in which the preamplifier Vcc voltage is provided directly from a system power supply, care must be taken that the system power supply have low output impedance and low noise.

The leads from the detector to the preamplifiers should be kept as short as possible. Because of the low impedance involved, the detector/preamp interface is not particularly sensitive to electrostatic pickup but care should be taken to minimize any fluctuating magnetic fields through judicious use

of magnetic shielding.

Also due to the low detector impedences, crosstalk due to finite impedance in detector common lead is a frequency problem. To minimize and localize this effect the Common Module detector brings out a common lead for each 5 detector elements. These common leads are totally independant. The signal current in the common and the impedence of the common is thereby reduced minimizing crosstalk and localizing any residual crosstalk within a group of 5 elements. Care must similarly be taken in the system wiring to maintain low impedence in the common and power ground wiring.

The on-board regulator of the preamplifier module is not current limited. Care must be taken during test and trouble shooting to avoid accidental shorting of the Vcc line as this will cause damage to the regulator.

The Ident resistors of the module serve to identify the module when tested by the Land Combat Support System (LCSS) an integrated test and maintenance facility. Connections to J1 pins 22 and 24 are not required for system operation.

Connections to pins 20 and J1 should <u>not</u> be made to the postamplifier. The corresponding pins on the postamplifier are connected to the postamplifier LCSS identification resistors. Pins 20 and 7 of J1 of the preamplifier should be used for test or monitoring purposes only.

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the Preamplifier Module. Presented herein are the test equipment requirements, and alignment techniques.

4.2 TEST EQUIPMENT

The following, or equivalent, test equipment is required to perform the necessary operational tests, alignments, adjustments on the Preamplifier.

4.2.1 STANDARD TEST EQUIPMENT

Table 4-1, following, presents a listing of commercially available equipment which has been found to be adequate for testing of this module.

TABLE 4-1

STANDARD TEST EQUIPMENT

Equipment	Manufacturer	Model
Oscilloscope	Tektronix	453
Digital VTVM	Fluke	4400
VOM	Simpson	260
VTVM	Hewlett-Packard	3400A
Power Supply (2)	Lambda	LPD4222FM
Function Generator	Wavetek	110

4.2.2 SPECIAL TEST EQUIPMENT

Two items of special test equipment are required to accomplish the module tests described herein. A switching and control unit, hereafter referred to as the test set, and a 40 dB wide band amplifier. This test equipment may be fabricated locally. Figure 4-1 and 4-2 provide schematic diagrams and information on fabrication.

The test set facilitotes mounting the module for test, allows easy channel selection, and provides convenient test points.

Although 40 dB amplifiersare available commercially, the fabricated compilfier provides the inherent low noise and minimal 60 Hz pick-up essential during Preamplifier noise measurements.

4.3 SPECIAL TOOLS

No special tools are required to test or align the Preamplifier module.

4.4 TEST SET UP

A typical test set up interconnection diagram is shown in Figure 4-3.

4.5 CALIBRATION PREPARATION FOR USE

In order to determine that the Preamplifier module meets its performance requirements, the following test sequence is recommended.

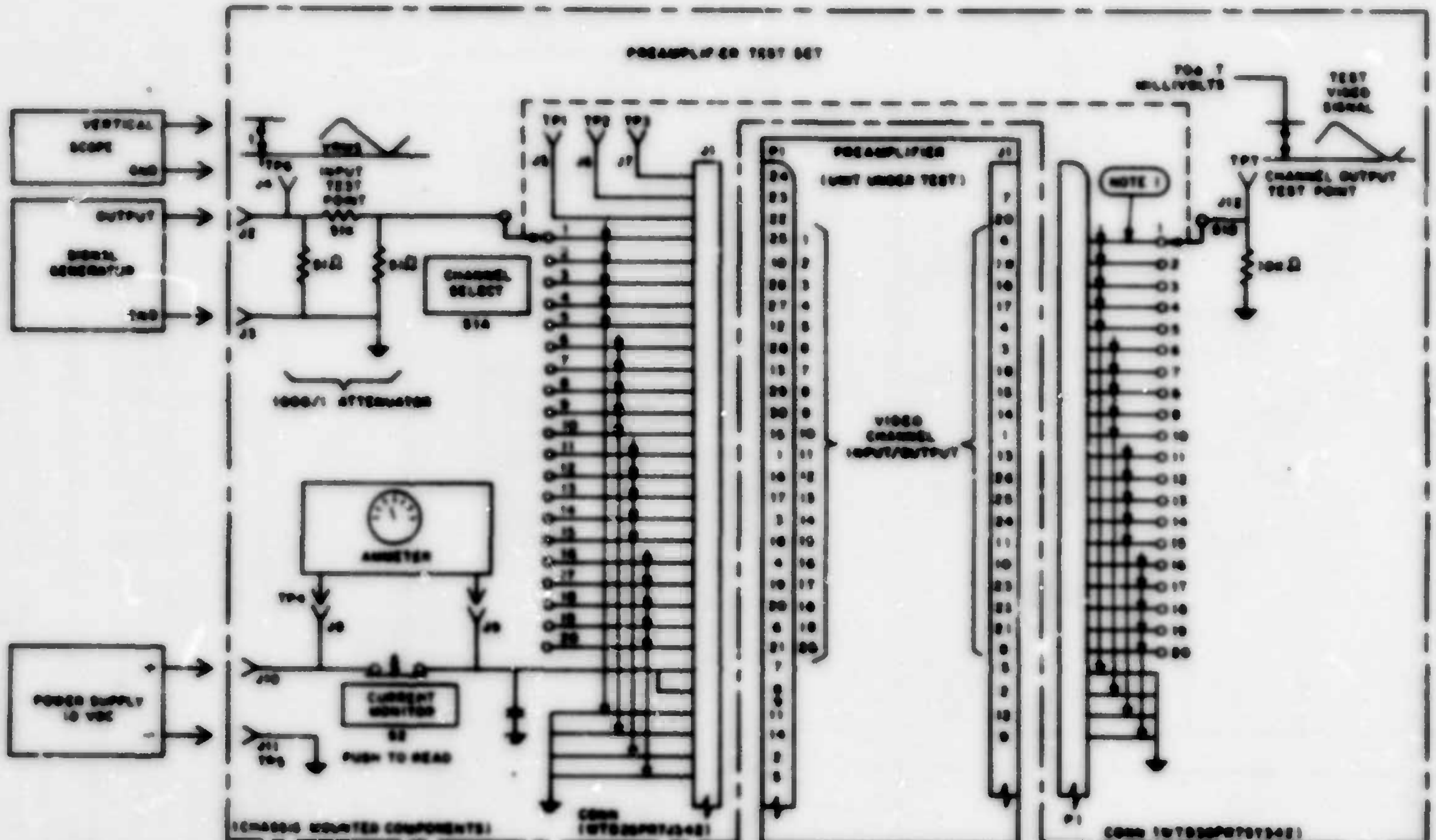
4.5.1 ELECTRICAL TESTS AND ADJUSTMENTS

Perform each test as specified in the following paragraphs in the order presented. As each action is completed, verify a proper response or indication before proceeding to the next action.

4.5.1.1 Equipment Interconnection

4.5.1.1.1 Connect the Preamplifier to the test set as shown in Figure 4-1.

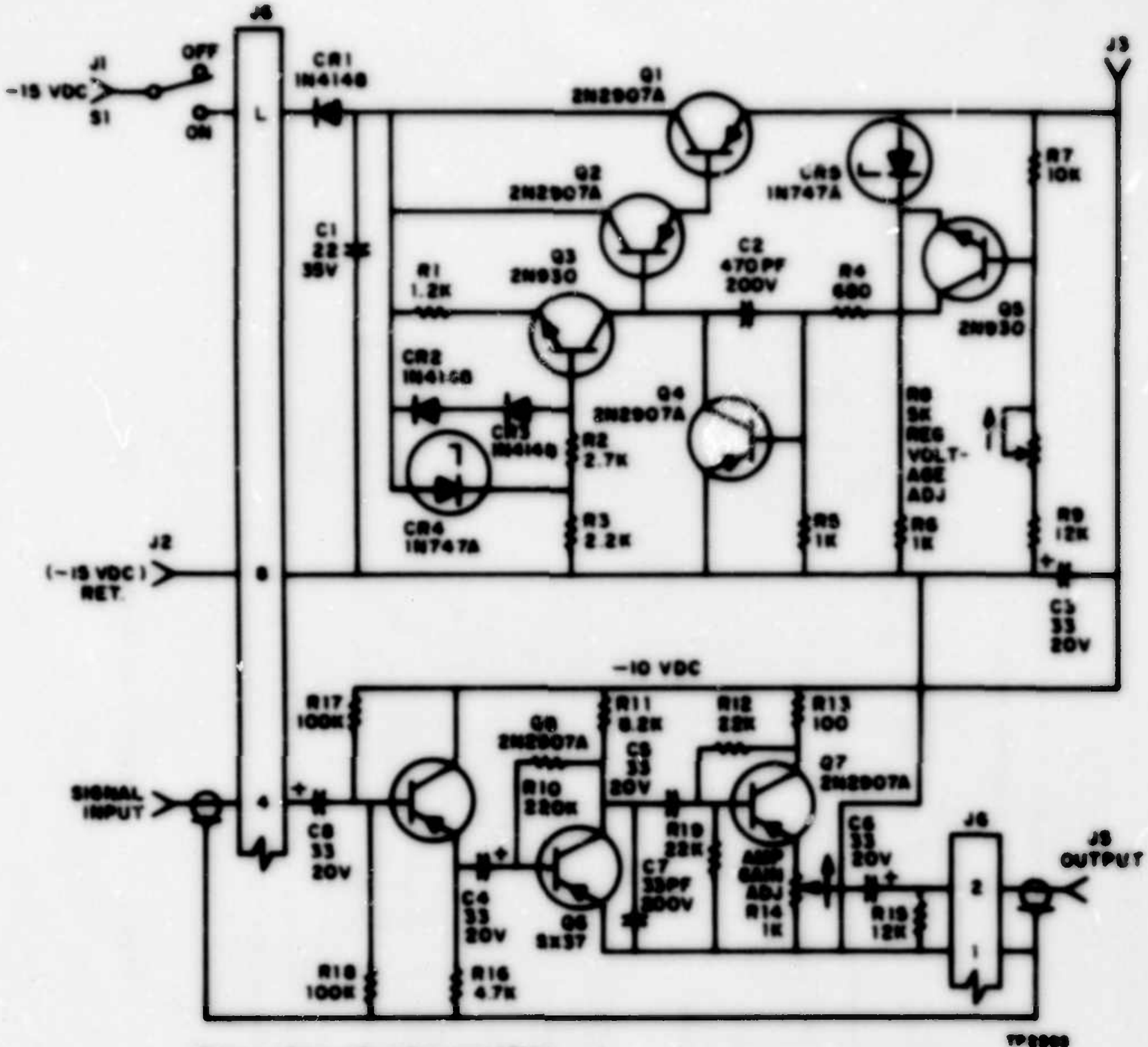
4.5.1.1.2 Interconnect the Test set and test equipment as shown in Figure 4-3.



NOTES:

2. ALL COMPONENTS OF TEST SET SHOULD BE MOUNTED IN METAL BOX

Figure 4-1 Preamplifier Module Test Set



Notes unless otherwise specified

1. Reference designation prefix 1.
2. Resistance values are in ohms.
3. Capacitors values are in microfarads.
4. Test set is used in measuring Common Module preamplifier equivalent input noise.
5. Functional test procedure.
   A. Energize test set with -15VDC from J1 to J2 and turn switch S1 on.
   B. Adjust R8 for a voltage of -10.0 ±0.05VDC at J3.
   C. Input A 1 MV RMS at 10 KHZ sine wave at J4 from a wavetek 110 or equivalent.
      (An external input resistor divider network of 51 K to 51 may be necessary).
   D. Monitor output J5 with an oscilloscope and an RMS voltmeter.
   E. Adjust R14 for an RMS voltage gain of 40 DB (Av= 100).
   F. Bandwidth check 10 HZ is -1 ±0.5 DB, flat from 30HZ to 75 KHZ, down -3 ±0.5 DB at 600 KHZ.

Figure 4-2 40dB Wideband Amplifier Schematic Diagram

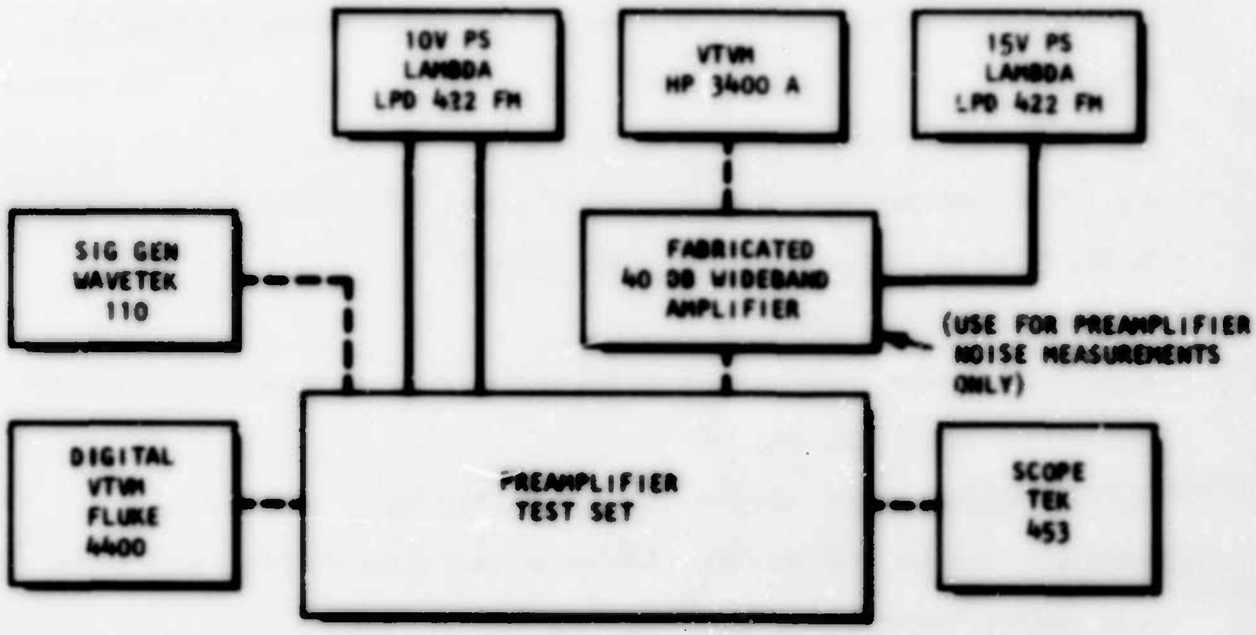


Figure 4-3 Test Setup, Preamplifier Noise Test

Do not include the 40 dB amplifier at this time.

4.5.1.1.3 Verify that all the above test set up interconnections are properly made.

4.5.1.1.4 Using an ohmmeter, measure the resistance between test points 1 and 2 on the test set.

The ohmmeter shall indicate 1K ohm, ±5%.

4.5.1.1.5 Using the ohmmeter, measure the resistance between test points 2 and 3.

The ohmmeter shall indicate 6.81K ohms ±5%.

4.5.1.1.6 Turn all test equipment on and adjust output of power supply to 10 Vdc ±0.5V as measured at test points 4 and 5.

4.5.1.2 Input Power Measurement

4.5.1.2.1 Measure input current to the preamplifier by momentarily depressing current monitor switch, S2.

The Ammeter shall indicate .055 Amps ±0.010 Amps.

4.5.1.2.2 Measure the regulated 3.6 Vdc at test point 2. Using test point 5 as ground. The voltmeter shall indicate 4.6 Vdc ±0.3 Vdc.

4.5.1.3 Voltage Gain and Bandwidth

4.5.1.3.1 Adjust the signal generator amplitude to provide a 1-volt RMS input signal at 1 kHz to test point 6. Input attenuator reduces the signal to the Preamplifier input to 1 millivolt.

NOTE: Midband voltage gain is given by $A_v = \frac{e_{out}}{e_{in}}$. Therefore aproximate voltage gain can be obtained easily by applying the 1 millivolt signal to a channel input and reading the channel output voltage (in millivolts) as the gain.

4.5.1.3.2 Set test set CHANNEL SELECT switch S_1 to position 1. Read channel output on the VTVM connected to test point 7.

Output voltage shall be 70 millivolt ±7 millivolts

4.5.1.3.3 Repeat paragraph 4.5.1.3.2 for switch position 2 through 20, corresponding to wider channels 2 through 20.

4.5 1.3.4 Return CHANNEL SELECT switch to position 1

4.5.1.3.5 Increase signal generator output frequency until VTVM indicates a 3 dB drop in amplitude at test point 7. (Reference: 0 dB at 1 kHz)

NOTE: The signal generator frequency dial indication.

Channel bandwidth shall be 105 kHz ±25 kHz.

4.5.1.3.6 Repeat paragraph 4.5.1.3.5 for channels 2 through 20.

4.5.1.4 Noise Measurement

4.5.1.4.1 Interconnect the 40 dB amplifier into test setup as shown in Figure 4-3.

4.5.1.4.2 With no input signal to the preamplifier test set, measure the true RMS output noise for each of the 20 preamplifier channels. A sufficient condition for acceptance is an output noise level of less than or equal to the maximum given in Table 4-2 for the respective channel gain and bandwidth.

NOTE: 60 Hz pickup must be minimized during the noise measurement.

4.5.2 MECHANICAL ALIGNEMENT

No unique mechanical alignment constraints are presented by the Preamplifier.

4.5.3 ADJUSTMENT IN THE SYSTEM

Preamplifier characteristics are determined and fixed by the components selected at design. No adjustment or alignment is needed upon installation.

4.6 SPECIAL MAINTENANCE REQUIREMENTS

The Preamplifier requires no special maintenance attention other than the routine procedures followed for general electronic equipment. No time change components are contained in this module.

MAX e_{out}, mv rms

Band-Width kHz ≥ \ A ≥	65	66	67	68	69	70	71	72	73	74	75	76	77
80	4.04	4.10	4.16	4.23	4.28	4.35	4.41	4.47	4.53	4.59	4.66	4.72	4.78
82	4.09	4.16	4.22	4.28	4.34	4.41	4.47	4.53	4.60	4.66	4.72	4.78	4.85
84	4.13	4.20	4.27	4.33	4.39	4.45	4.52	4.58	4.65	4.72	4.77	4.83	4.90
86	4.18	4.24	4.31	4.37	4.43	4.50	4.57	4.63	4.69	4.75	4.82	4.83	4.95
88	4.24	4.30	4.37	4.43	4.50	4.56	4.63	4.69	4.76	4.82	4.89	4.95	5.02
90	4.28	4.35	4.42	4.48	4.55	4.62	4.68	4.75	4.82	4.88	4.95	5.02	5.08
92	4.33	4.40	4.46	4.53	4.59	4.66	4.73	4.80	4.86	4.93	5.00	5.07	5.13
94	4.37	4.44	4.52	4.57	4.64	4.71	4.78	4.85	4.91	4.98	5.05	5.12	5.18
96	4.42	4.48	4.55	4.62	4.69	4.76	4.83	4.89	4.96	5.03	5.10	5.16	5.23
98	4.47	4.53	4.60	4.67	4.74	4.81	4.88	4.95	5.01	5.08	5.15	5.22	5.28
100	4.51	4.58	4.65	4.72	4.78	4.86	4.93	5.00	5.07	5.13	5.20	5.27	5.34
102	4.56	4.63	4.70	4.77	4.84	4.91	4.98	5.05	5.12	5.19	5.26	5.34	5.41
104	4.61	4.68	4.75	4.82	4.09	4.96	5.03	5.10	5.17	5.24	5.31	5.39	5.46
106	4.65	4.73	4.80	4.87	4.94	5.02	5.08	5.16	5.23	5.30	5.37	5.45	5.52
108	4.70	4.78	4.84	4.92	4.99	5.06	5.13	5.21	5.28	5.35	5.42	5.50	5.57
110	4.74	4.82	4.88	4.96	5.03	5.10	5.17	5.25	5.33	5.39	5.46	5.54	5.62
112	4.78	4.86	4.92	5.00	5.07	5.14	5.21	5.29	5.37	5.44	5.51	5.59	5.67
114	4.82	4.89	4.97	5.04	5.12	5.19	5.26	5.34	5.41	5.49	5.56	5.64	5.71
116	4.86	4.93	5.01	5.09	5.16	5.24	5.31	5.39	5.46	5.54	5.61	5.69	5.76
118	4.91	4.98	5.06	5.14	5.21	5.28	5.36	5.44	5.51	5.58	5.66	5.74	5.81
120	4.95	5.02	5.10	5.19	3.25	5.33	5.41	5.49	5.56	5.63	5.71	5.79	5.86

Table 4-2 Noise Level Outputs

CHAPTER 3

POSTAMPLIFIER/CONTROL DRIVER,

VIDEO, INFRARED

USAECOM SM-D-773900

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Infrared Video Postamplifier/Control Driver module, hereinafter called the postamplifier, provides the amplification and signal conditioning functions required of a Common Module infrared imaging system. In a standard common module system the signals from the detector are processed through a stage of preamplification and then fed to the postamplifier module. Each postamplifier module processes 20 channels of information. Each channel consists of two amplifier/control stages and a light emitting diode (LED) driver stage. The implementation uses 12 dual-in-line IC packages with three packages series connected and 4 packages in parallel with 5 channels in each IC package.

1.2 INTENDED USE OF ITEM

The postamplifier module has been designed to be interfaced with other major common and special modules to form an integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The function of the postamplifier is to provide additional amplification and processing of signals received from preamplifier common modules. After amplification and other processing, the postamplifier final stage provides the drive voltages required by the LED array.

1.3 TECHNICAL SPECIFICATIONS

The technical specifications of the postamplifier module are as follows:

Parameter	Specification
Voltage Gain	Programable From 10,000 to 18,000 V/V as follows: P1-12 Gain Command 1 controls A1-A4AR1 P1-29 Gain Command 2 controls A1-A4AR2

Parameter	Specification
Gain Control	0 to 30 dB
Bandwidth	
Upper 3dB Frequency	110 ± 40 kHz
Lower 3dB Frequency	6 ± 2 Hz
Flat (± 0.5 dB to midband gain) (Midband gain reference: 0dB at 1 kHz)	30 Hz to 30 kHz
Input Impedence	7500 to 12,500 ohms (10,000 nominal)
Output Impedence	195 to 215 ohms (205 Ω nominal)
Output Current	10 ± 3mA peak into 390 Ω in series with LED.
Polarity Control	Output in phase or 180° out of phase with input.
Recovery Time (From 1 volt, 50 msec step input)	0.2 seconds
AC Gain Balance Range	15 dB minimum

Power Requirements	Low Power	High Power	Ripple (mVrms)
Pins P1-32, 17, 2, 23	+4.8 @ 15mA	+10 @ 35mA	100
P1-10	-4.8 @ 30mA	-6, -7.5 @ 35mA	Hi-100, Lo-50
P1-30	+7 @ 30mA		
P1-27	-3.5 @ 35mA	-4.25 @ 45mA	0.2
P1-11	+3.5 @ 35mA	+4.25 @ 45mA	0.2

NOTE:

For mechanical specifications involved with interface requirements such as mechanical configuration, interconnection, and mounting information, refer to section III.

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The postamplifier module is comprised of twelve integrated circuits (IC's) on a printed wiring board. Each postamplifier module processes 20 channels of information. Each channel consists of two amplifier/control stages and a light emitting diode (LED) driver stage. The implementation uses 12 dual-in-line IC packages with three packages series connected and 4 packages in parallel with 5 channels in each IC package. The arrangement can be seen in the schematic of Figure 2-1.

The first and second stage provides an electronically controlled gain variation of 30db. Each of the two stages is capable of providing a polarity (phase) reversed function to provide a white/hot-white cold image but the module wiring is such that only the second stage is used for polarity reversal. As can be seen on the schematic, potentiometers between the first two stages are provided to adjust channel gain to compensate for variations in detector responsivity. The final LED driver stage provides the current drive to the LED module to give a light intensity output proportional to signal level.

2.2 THEORY OF OPERATION

Each gain/polarity control IC stage shown in the schematic of Figure 2-2 consists of three differential amplifiers. Gain control is accomplished by controlling the current source to the input differential. The other two differential amplifiers are connected in parallel. Polarity reversal is accomplished by turning one or the other transistor pair on and off. A zero (ground) input to the polarity control point provides inverting gain while

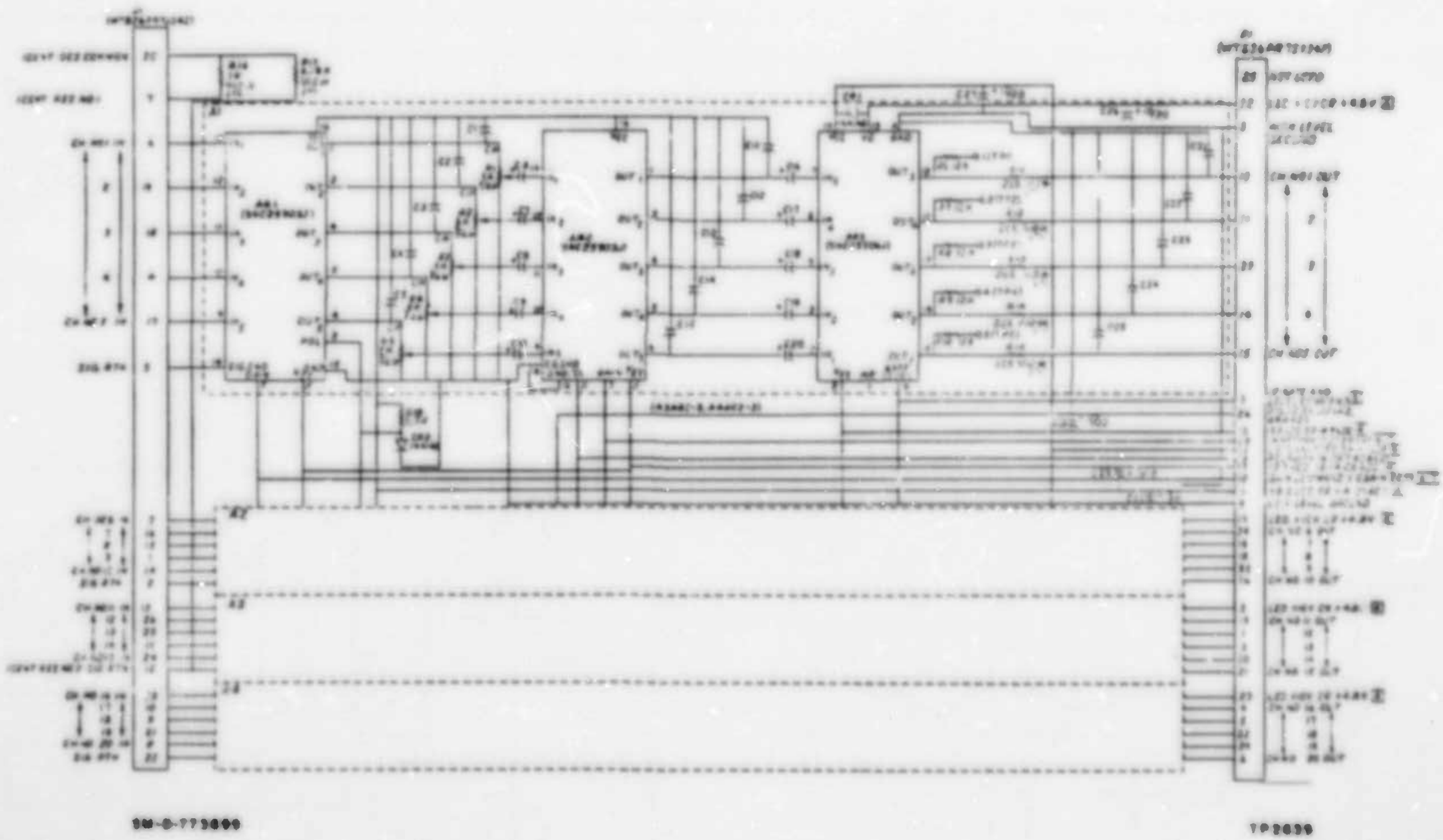
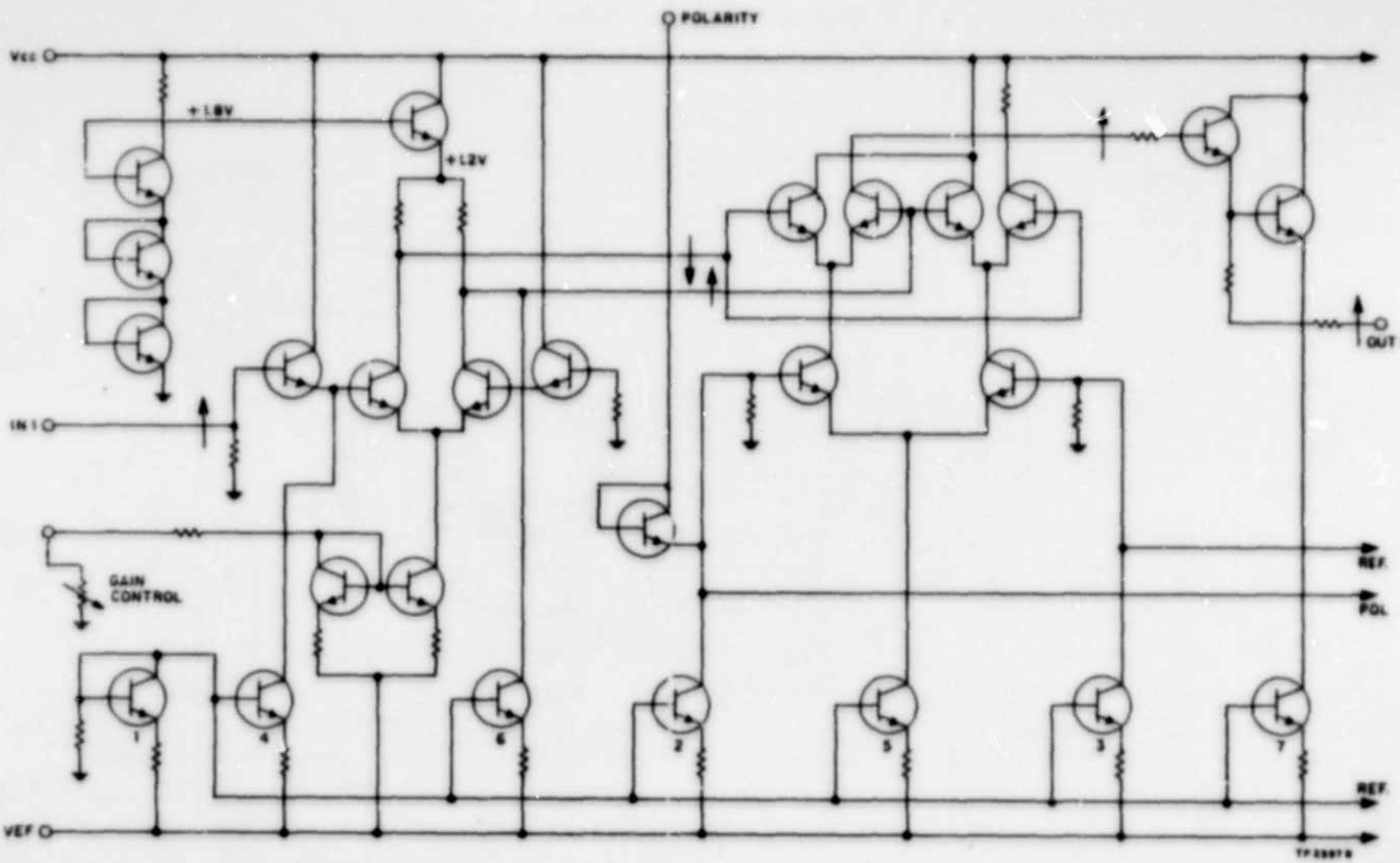


Figure 2-1. Postamplifier Schematic Diagram



TP2615

Figure 2-2 Postamplifier Video Control IC Schematic Diagram

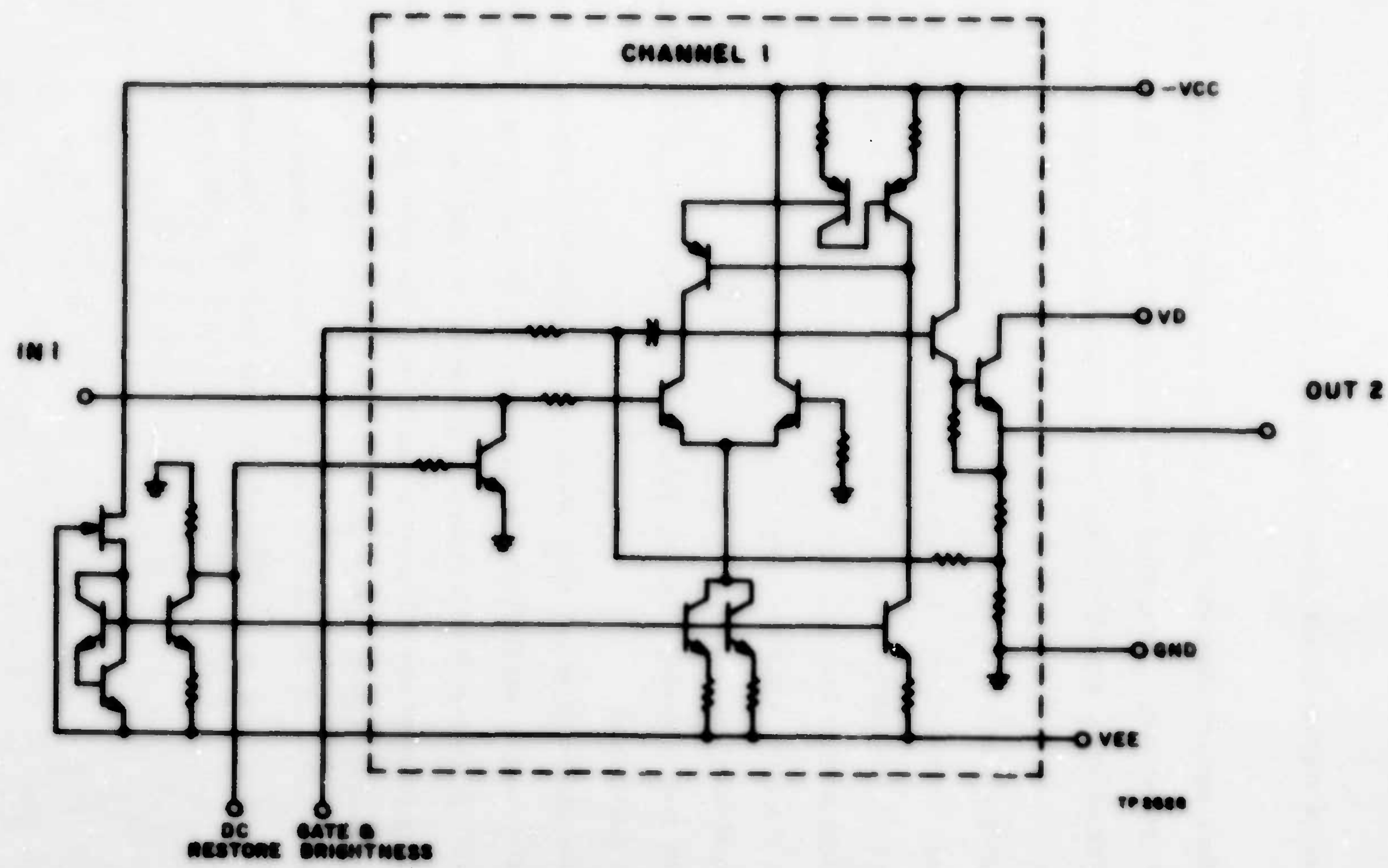


Figure 2-3. Postamplifier Module LED Driver IC Schematic Diagram

a negative voltage to the polarity control point provides noninverting gain.

Gain control commands 1 and 2 control the gains of the first and second stage respectively. In combination a gain control range of 30 dB is achieved.

The polarity command voltage and the inverse polarity command voltage can be fed to two separate input pins on the module. Thus it is possible for 10 amplifiers on the module to be operated inverting and the other 10 be operated noninverting. This connection can be used when a dual bias regulator is used to bias half the detector elements with a positive bias and the other half with a negative bias. This arrangement has the advantage of equal loading of the power supplies, power supply busses and commons on each module. When a single bias regulator is used a single polarity control line is used and the input connector pins are jumped to supply the same polarity command to all amplifiers.

The final LED driver stage shown in the schematic of Figure 2-3 consists of a differential amplifier and a two transistor follower stage. Negative feedback is supplied from a resistive divider in the follower stage to the inverting input of the differential amplifier. The video gate and brightness level signals are also summed into the non-inverting input. Voltage gain is set by the ratio of the feedback resistor and the resistance of the input summing network and is approximately 6. The input also has a transistor clamp for DC restoration.

SECTION III

INTERFACE

3.1 CONFIGURATION

Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating the Postamplifier module in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is a photograph of the module and Figure 3-3 is a parts location drawing.

3.2 INTERCONNECTING INFORMATION

The input signals are received through J1 from a cable which interconnects with the output of the Preamplifier module. Output signals, input power and input commands pass through P1 to a connector on a mother board or wiring harness. Each end of the module must be supported by a suitable mounting slide. For applications involving severe shock or vibration, positive means should be provided to retain the module in the fully engaged position and also to retain the cable connector which engages with J1. Access must be provided for the test points and for adjustment of the trim potentiometers at the top of the module.

3.3 THERMAL DESIGN CONSIDERATIONS

Although the individual Postamplifier Module power dissipation is only 1.67 watts per module, very small in an overall system, it must be taken into account during system design. Refer to Section III of Chapter 1, for a detailed discussion of the system thermal design considerations.

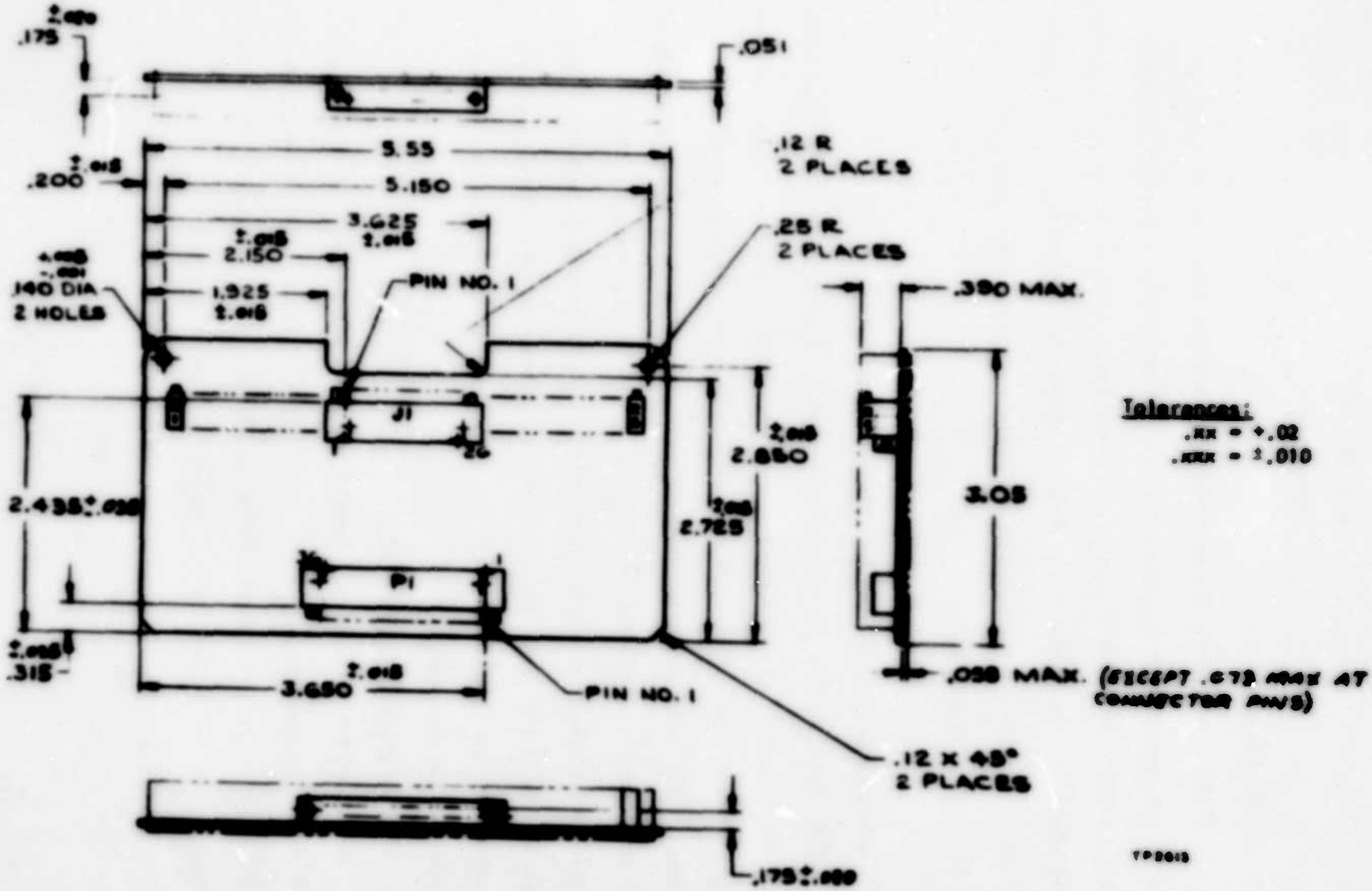


Figure 3-1 Postamplifier Module Outline Drawing

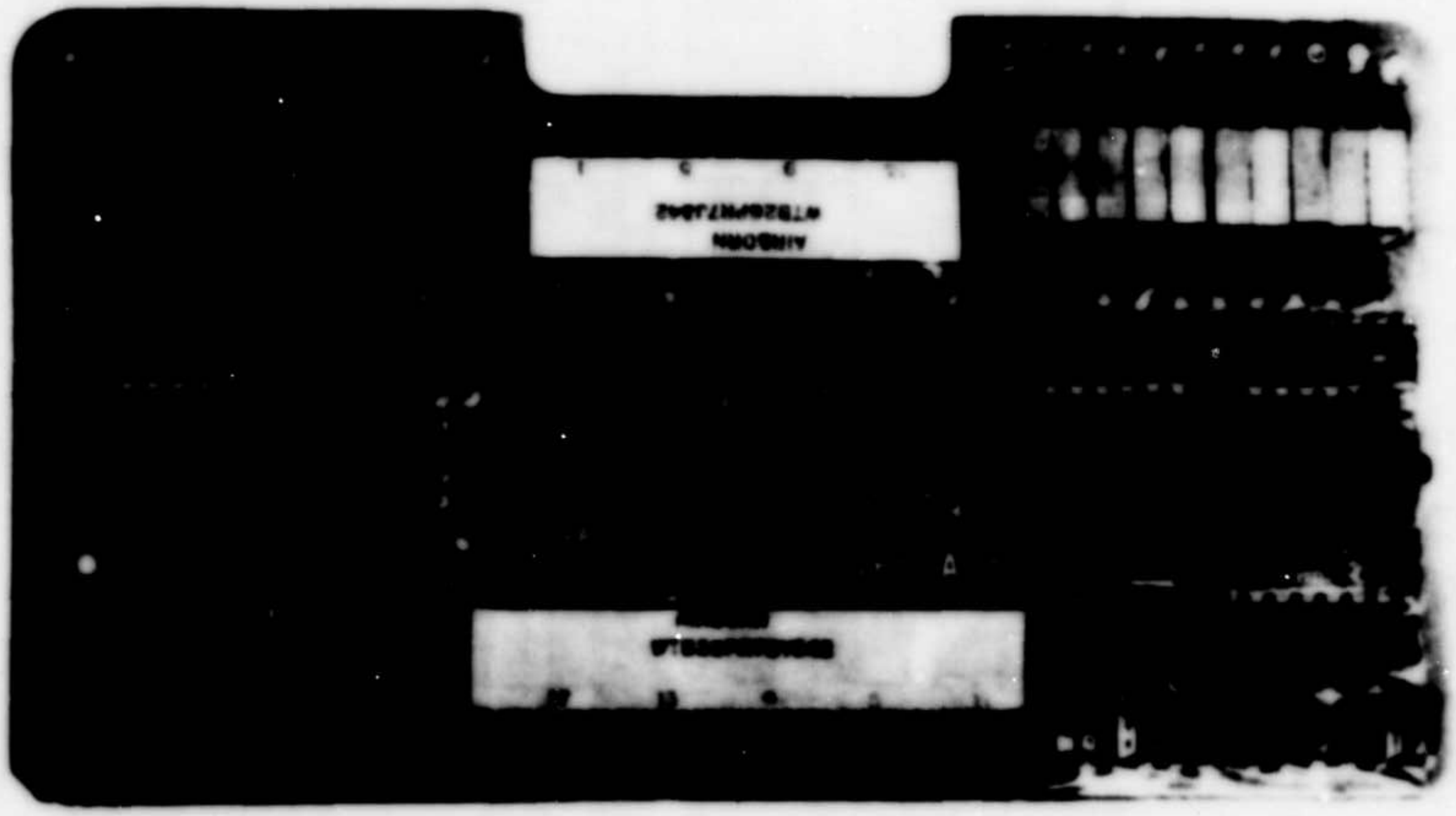
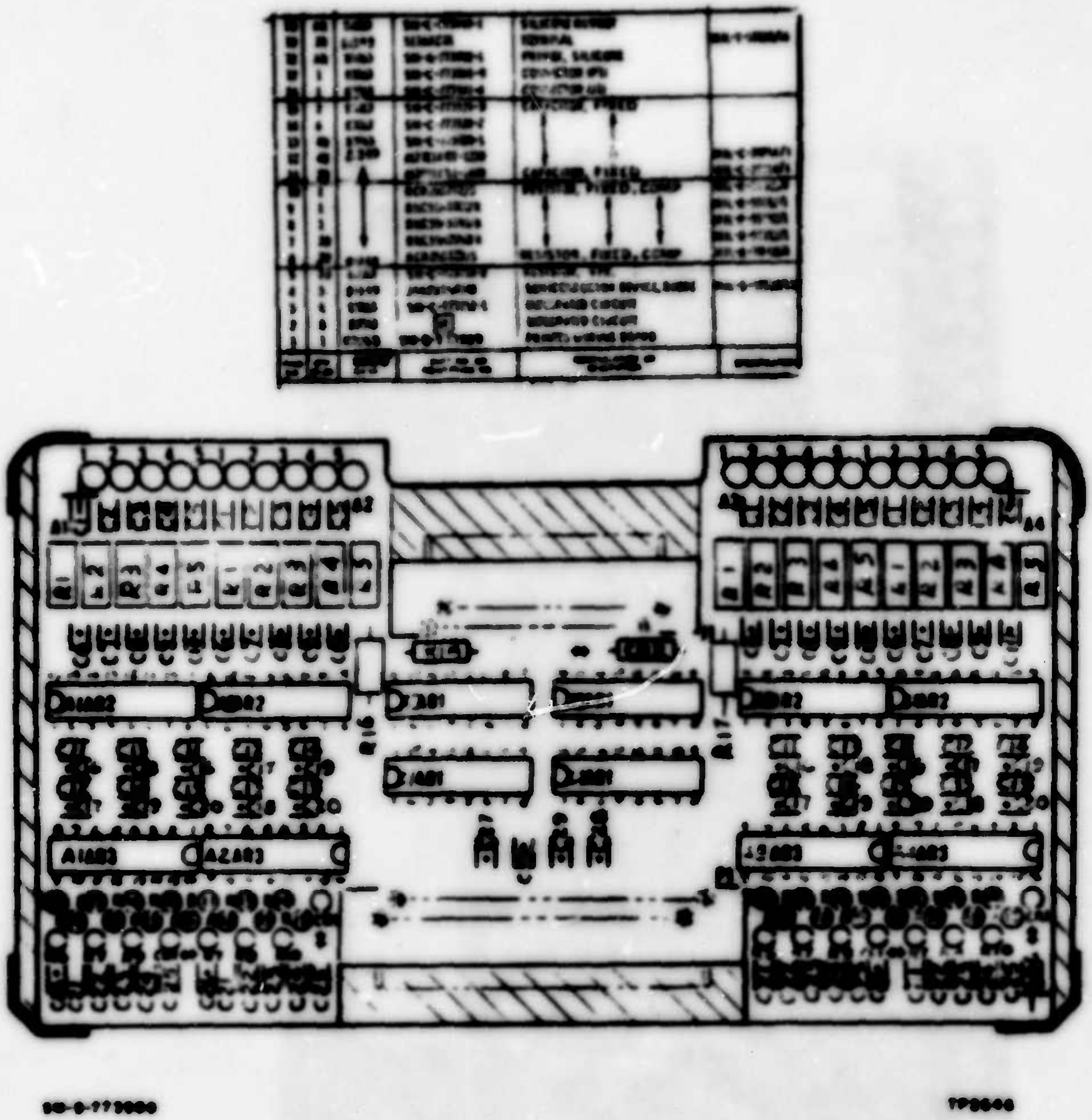


Figure 3-8. Photo of Postamplifier Module

TP8018



NOTE: Reference designations for each nonremovable identical stage are assigned by prefixing with A1-A4
Example: C1 is A5GA1C1 on Stage A1
C1 is A5GA2C1 on Stage A2
C1 is A5GA3C1 on Stage A3
C1 is A5GA4C1 on Stage A4

Figure 3-3. Postamplifier Module Parts Location Drawing

3.4 ELECTRICAL INTERFACE DATA

3.4.1 INPUT CHARACTERISTICS

(a) Impedance: 7500 to 12,500 ohms

(b) Voltage/Current/Ripple:

Low-power application

P1 Pin No.	Voltage (Vdc nominal)	Current (Idc nominal)	Maximum Ripple Voltage (± mV rms)
32	+4.8	0.015 average	100
17	+4.8	0.015 "	100
2	+4.8	0.015 "	100
23	+4.8	0.015 "	100
10	-4.8	0.030	100
30	+7.0	0.030	100
27	-3.5	0.035	0.2
11	+3.5	0.035	0.2

High-power application

P1 Pin No.	Voltage (Vdc nominal)	Current (Idc nominal)	Maximum Ripple Voltage (± mVrms)
32	+10.0	0.035 average	100
17	+10.0	0.035 average	100
2	+10.0	0.035 average	100
23	+10.0	0.035 average	100
10	-6, -7.5	0.035	50
30	disc.	—	—
27	-4.25	0.045	0.2
11	+4.25	0.045	0.2

3.4.2 OUTPUT CHARACTERISTICS

(a) Impedance: 195 to 215 ohms

(b) Voltage gain: Programmable from 10,000 to 18,000 volts per volt

(c) Gain control: range 0 to 30 dB minimum

(d) Current (High-power application): 10 ±3 milliamperes peak into load consisting of a 390 ohm resistor in series with an LED

(e) Polarity: polarity function provided allows output to be in phase or 180° out of phase with input signal

3.4.3 PROCESSING CHARACTERISTICS

(a) Signal bandwidth: with a load consisting of a 390 ohm resistor in series with a light-emitting diode, upper

3dB frequency 110 ±40 kHz; lower 3dB frequency 6 ±2 Hz; gain-flat (±0.5dB of midband gain) from 30 Hz to 30 kHz (midband gain reference: 0dB at 1 kHz)

(b) Recovery time: ∠0.2 second from a 1 volt, 50 millisecond step input representing a blast to display a projectile signal at the postamplifier output with an input amplitude of 50 millivolts

NOTE:

Recovery time is measured from trailing edge of step input

(c) AC gain balance: variable resistor provided in each postamplifier channel which allows 15 dB minimum ac gain balance range to balance variations in detector responsivity to amplifier gain variations

(d) Channel-to-channel tracking: maximum variation in voltage gain of each channel is ±5% of average gain on 20 channel postamplifier over temperature range of 0° to +55°C; provides specified tracking without readjustment of channel gain controls over specified temperature range; tracking error is ≦ ±10% over temperature ranges of +71° to +55°C and 0° to -54°C

(e) Voltage gain drift: maximum variation in average voltage gain of 20 channels on each postamplifier is ±10% of average gain at ambient, over operating temperature range of 0° to +71°C and ±15% of average gain at ambient, over operating temperature range of -54° to 0°C

(f) Gain tracking error: Channel-to-channel gain tracking error is within ± 5% over gain control range (30dB minimum) at ambient temperature; gain tracking error is ≦ ±5% over temperature range of +55° to 0°C and is ≦ ± 10% over temperature ranges of +55 to 71°C and 0° to -54°C

3.4.4 ANCILLARY ELECTRICAL DESIGN CONSIDERATIONS

(1) Since no maximum input signal amplitude nor percent output distortion for different input signal amplitudes are specified, the maximum input signal amplitude for an allowable percent output distortion should be determined prior to its system use.

3dB frequency 110 ±40 kHz; lower 3dB frequency 6 ±2 Hz; gain-flat (±0.5dB of midband gain) from 30 Hz to 30 kHz (midband gain reference: 0dB at 1 kHz)

(b) Recovery time: $\angle$0.2 second from a 1 volt, 50 millisecond step input representing a blast to display a projectile signal at the postamplifier output with an input amplitude of 50 millivolts

NOTE:

Recovery time is measured from trailing edge of step input

(c) AC gain balance: variable resistor provided in each postamplifier channel which allows 15 dB minimum ac gain balance range to balance variations in detector responsivity to amplifier gain variations

(d) Channel-to-channel tracking: maximum variation in voltage gain of each channel is ±5% of average gain on 20 channel postamplifier over temperature range of 0° to +55°C; provides specified tracking without readjustment of channel gain controls over specified temperature range; tracking error is ≲ ±10% over temperature ranges of +71° to +55°C and 0° to -54°C

(e) Voltage gain drift: maximum variation in average voltage gain of 20 channels on each postamplifier is ±10% of average gain at ambient, over operating temperature range of 0° to +71°C and ±15% of average gain at ambient, over operating temperature range of -54° to 0°C

(f) Gain tracking error: Channel-to-channel gain tracking error is within ± 5% over gain control range (30dB minimum) at ambient temperature; gain tracking error is ≲ ±5% over temperature range of +55° to 0°C and is ≲ ± 10% over temperature ranges of +55 to 71°C and 0° to -54°C

3.?.4 ANCILLARY ELECTRICAL DESIGN CONSIDERATIONS

(1) Since no maximum input signal amplitude nor percent output distortion for different input signal amplitudes are specified, the maximum input signal amplitude for an allowable percent output distortion should be determined prior to its system use.

(2) The maximum brightness light emitting diode (LED) display will be obtained using "high power system" supply voltages, i.e., nominal voltages of +4.25, +10.0, -4.25 and -7.5 volts dc, capable of supplying a total of 2.05 watts. If power is a significant design constraint, the "low power system" supply voltages should be used, i.e., nominal +3.5, +4.8, +7.0, -3.5 and -4.8 volts dc capable of supplying a total of 0.77 watt. The use of "low power system" supply voltages, however, will result in a less bright display. The detailed input power requirements are described in 3.4.2.

(3) To avoid cross talk, input channel signal leads should not be bundled together. In addition, to avoid extraneous pick up, the input channel signal leads should be kept away from other high amplitude and or high frequency signal sources.

(4) The specified input impedance of 10,000 ohms nominal, and the specified output impedance of 205 ohms nominal are only valid at 1 kilohertz. At other frequencies, the impedance values will change accordingly.

(5) The "Polarity", "Video OFF Time", Video ON Time", "IR Gate and Level Command" and "Gain Command" operations, functions of the Post-amplifier/Control Driver, can be programmed by means of outputs provided by another Common Module, such as the Auxiliary Control, Video (see Chapter 4).

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the Postamplifier/Control Driver Module. Presented herein are the test equipment requirements, test set-up, adjustment and alignment techniques.

4.2 TEST EQUIPMENT

The following, or equivalent test equipment is required to perform the necessary operational tests, alignments, adjustments on this module.

4.2.1 STANDARD TEST EQUIPMENT

Table 4-1, following, presents a listing of commercially available equipment which has been found to be adequate for testing of the Postamplifier.

Table 4-1

STANDARD TEST EQUIPMENT

EQUIPMENT	MANUFACTURER	MODEL
Signal Generator	Wavetek	110
VOM	Simpson	260
Oscilloscope	Tektronics	453
VTVM	Hewlett-Packard	3400A
Power supply (5 required)	Lambda	LPD 422F4

4.2.2 SPECIAL TEST EQUIPMENT

In order to provide a convenient means of interconnecting the various equipment used in testing the Postamplifier, a control unit or test set is required. Such a test set may be fabricated from the information in Figure 4-1.

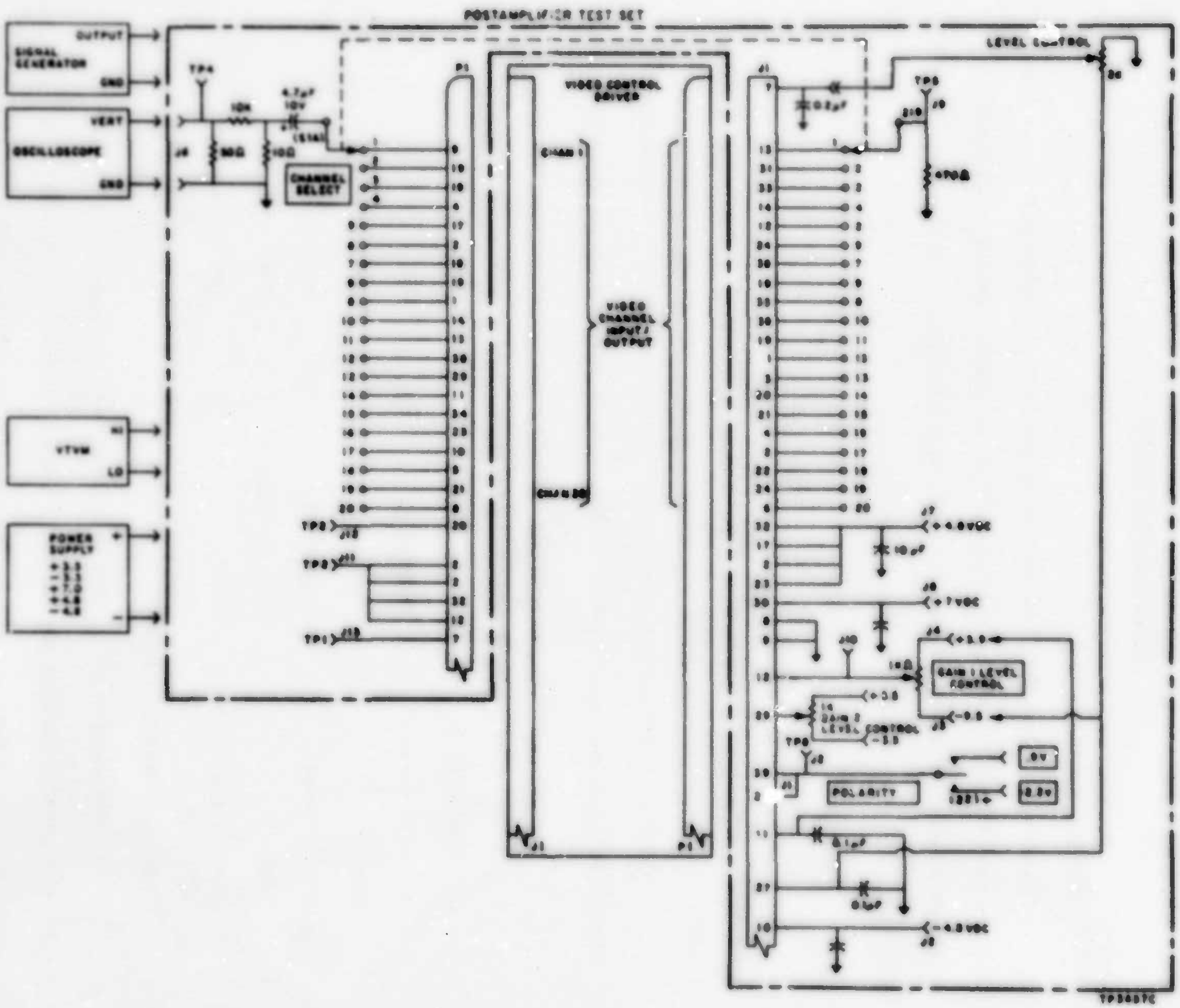


Figure 4-1. Postamplifier Test Set

4.3 SPECIAL TOOLS

No special tools are required to test the Postamplifier.

4.4 TEST SET UP

Figure 4-2 is a typical interconnection diagram.

4.5 CALIBRATION PREPARATION FOR USE

In order to determine that the Postamplifier module meets its performance requirements, the following test sequence is recommended.

4.5.1 ELECTRICAL TESTS AND ADJUSTMENTS

Perform each test as specified in the following paragraphs in the order presented. As each action is completed verify a proper response or indication before proceeding to the next action.

4.5.1.1.1 Connect the Postamplifier module to the test set as shown in Figure 4-1.

4.5.1.1.2 Interconnect the test set and test equipment as shown in Figure 4-2. Initial connection of the VTVM shall be to TP 4.

4.5.1.1.3 Verify that all the above connections are properly made.

4.5.1.1.4 Using an ohmmeter, measure the resistance between test points 1 and 3. The ohmmeter indication shall bu 1 K ohm ± .02 K ohm.

4.5.1.1.5 Measure for resistance between test points 2 and 3. The resistance shall be 6.19 K ohm ± 0.12 K ohm.

4.5.1.1.6 Turn on all test equipment and adjust power supply outputs as follows:

- 3.5 VDC ± 0.1V	- 4.8 VDC ± 0.1V
+ 3.5 VDC ± 0.1V	+ 4.8 VDC ± 0.1V
	+ 7.0 VDC ± 0.1V

4.5.1.2 Input Power Measurement

4.5.1.2.1 Measure the current being drawn from each of the supplies by the postamplifier.

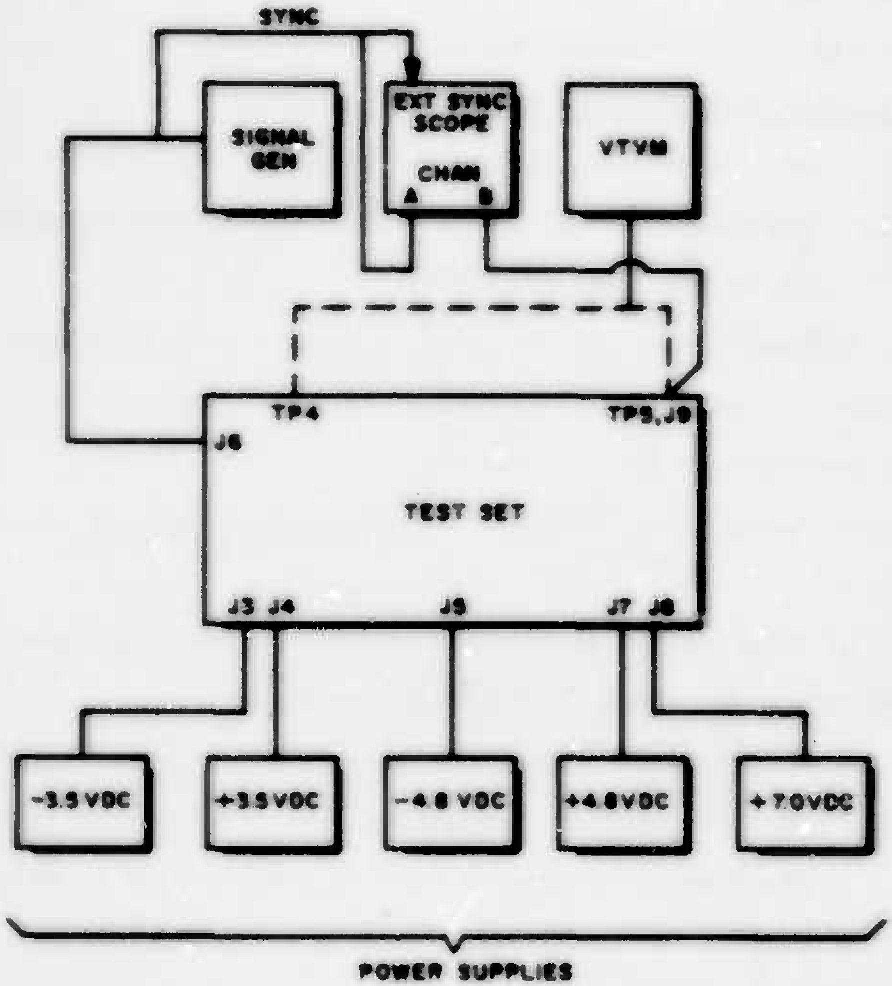


Figure 4-2. Postamplifier Test Setup

The current drawn shall be within the following limits:

Voltage	Current	Voltage	Current
- 3.5 V	40 ma ± 10 ma	- 4.8V	30 ma ± 10 ma
+ 3.5 V	40 ma ± 10 ma	+ 4.8V	110 ma ± 40 ma
		+ 7.0V	30 ma ± 10 ma

4.5.1.3 Voltage Gain Test

4.5.1.3.1 Adjust the GAIN BALANCE potentiometer, Figure 4-3, fully clockwise (maximum gain) on each of the 20 channels.

4.5.1.3.2 Adjust gain level on test set fully clockwise.

4.5.1.3.3 Adjust the signal generator output to provide an input signal of 30 millivolts at 1 kHz to test point 4 (Figure 4-1).

4.5.1.3.4 Set the test set CHANNEL SELECT switch to position 1. Read channel output on the VTVM connected to test point 5, J9.

Channel output voltage shall be no less than 378 millivolts.

NOTE

An output voltage reading of 420 mV rms is equivalent to a voltage gain of 18,000 volts per volt. The maximum voltage gain of each channel is given by

$$A_v = \frac{e_{out}}{e_{in}} \times 999 \times 1.43$$

The test set input resistor division ratio is 999 to 1 and the output resistor division ratio is 1.43 to 1.

4.5.1.3.5 Repeat paragraph 4.4.1.3.4 for channels 2 through 20.

4.5.1.3.6 Return CHANNEL SELECT switch to position 1.

4.5.1.4 Gain Control Range

In order to determine the individual gain range of each channel proceed as follows:

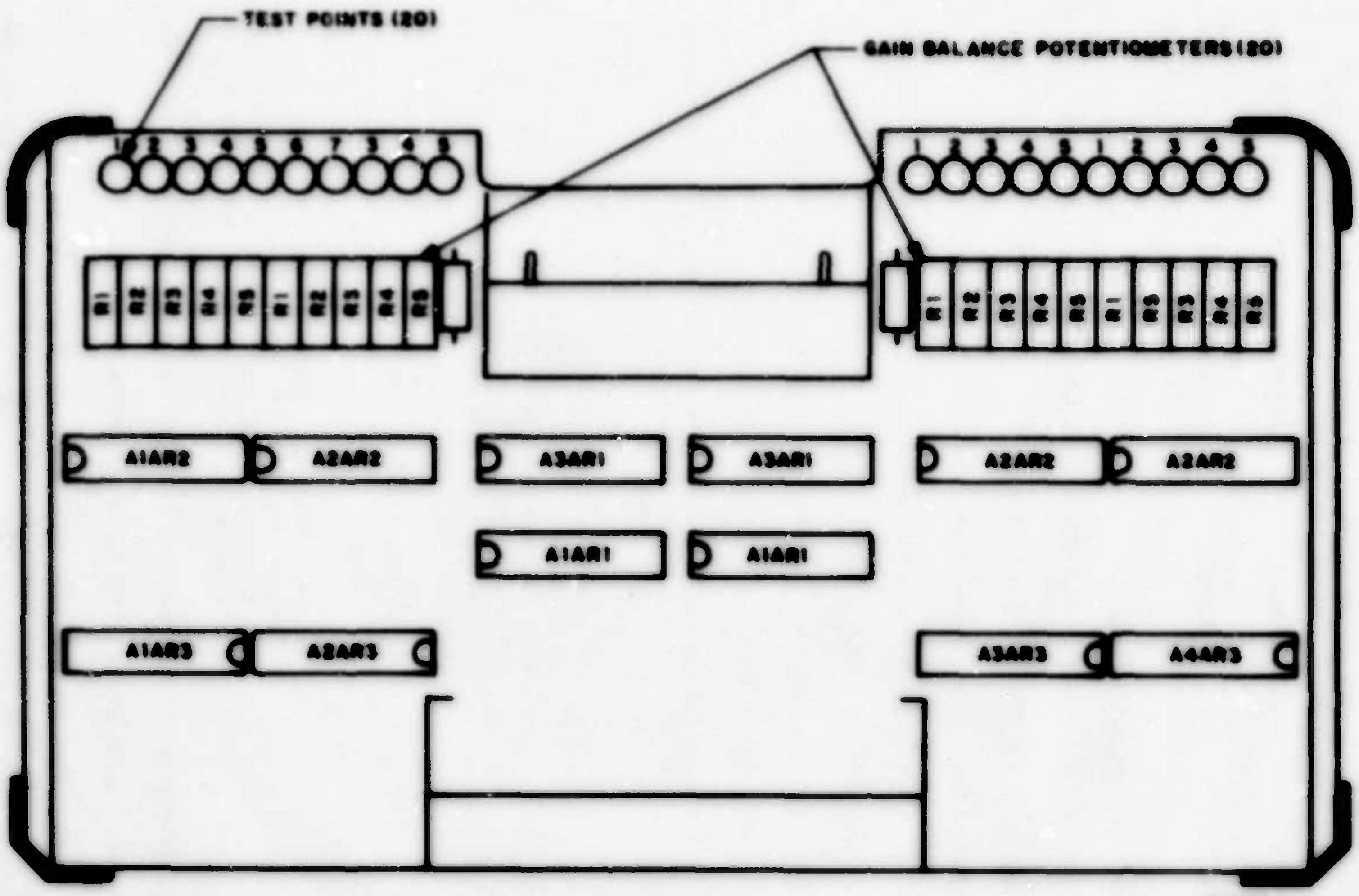


Figure 4-3. Postamplifier Test Points and Gain Balance Potentiometers

4.5.1.4.1 With the CHANNEL SELECT switch in position 1, and the Postamplifier Channel 1 GAIN BALANCE potentiometers fully clockwise, note the output voltage reading on the VTVM connected to TP 5. Adjust the GAIN LEVEL potentiometer fully counter-clockwise.

The output voltage shall decrease by 30 db minimum.

4.5.1.4.2 Repeat paragraph 4.4.1.4.1 for channels 2 through 20.

4.5.1.5 <u>Channel Bandwidth</u>

Connect a DC Voltmeter between J 10 and ground. Adjust the test set GAIN LEVEL control for 0.0 V dc.

4.5.1.5.2 Check signal generator output at test point 4. Readjust to 30 millivolts if necessary.

4.5.1.5.3 Set the test set CHANNEL SELECT switch to position 1. Increase the signal generator output frequency until the VTVM at test point 5 indicates an output voltage decrease of 3 db. (.707 of the level at 1 kHz).

The channel bandwidth shall be 110 kHz ± 40 kHz.

4.5.1.5.4 Repeat paragraph 4.4.1.5.4 for channels 2 through 20.

4.5.1.6 <u>Polarity Test</u>

4.5.1.6.1 Assure that oscilloscope channel A is connected to TP 4, channel B to TP 5. The oscilloscope is to be externally synchronized with the Postamplifier input signal.

4.5.1.6.2 Set the test set CHANNEL SELECT switch to position 1. Set test set POLARITY switch to POSITIVE position. Observe oscilloscope display of Postamplifier input signal, TP 4, and output signal TP 5.

The input signal and output signal shall be out of phase. Verify phasing of channels 2 through 20.

4.5.1.7 Output Noise Voltage

4.5.1.7.1 Adjust GAIN LEVEL on the test set fully clockwise.

4.5.1.7.2 Set test set POLARITY switch to POSITIVE.

4.5.1.7.3 Remove all connections from test set input.

4.5.1.7.4 With the VTVM connected to test point 5, measure the noise voltage output of channels 1 through 20.

The output noise voltage shall be equal to or less than 150 millivolts.

4.5.1.8 Test Point Continuity

4.5.1.8.1 Connect signal generator to test set input and adjust generator output to provide an input signal of 30 millivolts at 1 kHz at test point 4.

4.5.1.8.2 Verify continuity of test point resistor and conductor by observing the output waveforms on the oscilloscope; using a scope probe momentarily attached to each of the 20 printed wiring board test points. (See Figure 4-3)

4.5.2 MECHANICAL ALIGNMENT

While no mechanical alignment is required for the Postamplifier; when system layouts are being considered, orientation of the module should allow ready access to the twenty (20) GAIN BALANCE potentiometers.

4.5.3 ADJUSTMENT IN THE SYSTEM

When installed in a system, the GAIN BALANCE potentiometers of the Postamplifier are adjusted to balance variations in detector element responsivity to amplifier channel gain variations. A typical procedure would be as follows:

4.5.3.1 With the Postamplifier module installed in a system, and the system non-operating; adjust all GAIN BALANCE potentiometers to the center of their range. Disable and lock the scanner in a fixed position.

4.5.3.2 Prepare an infrared target of sufficient size and temperature such as to

cause the radiated energy to impinge upon each detector element completely and uniformally. Provide a "chopper wheel" to modulate the signal.

4.5.3.3 Energize the system. Using an oscilloscope and probe, observe the output at each of the test points on the Postamplifier. As an alternate method a test set may be fabricated to allow simultaneous viewing of the outputs by connecting the outputs to multiplexing circuitry synchronized to system clock frequency.

4.5.3.4 Depending on the particular system requirements, adjust each of the GAIN BALANCE potentiometers to equalize the outputs, e.g., establish a "line of balance" approximately 8 db between the highest and lowest channel. Adjust all outputs to this line. This will allow for additional future trim adjustments.

4.6 <u>SPECIAL MAINTENANCE REQUIREMENTS</u>

The Postamplifier module requires no special maintenance attention other than the routine procedures followed for general electronic equipment. No time change components are contained in this module.

CHAPTER 4

AUXILIARY CONTROL, VIDEO, INFRARED

USAECOM SM-D-773896

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Infrared Video Auxiliary Control module, hereinafter called the auxiliary control, provides video signal control functions for a common module infrared system. These control functions regulate infrared signal gain, amplitude and polarity. The module also provides positive and negative voltage regulators, scan failure protection and polarity transient suppression.

1.2 INTENDED USE OF ITEM

The auxiliary control module has been designed to interfaced with other major common and special modules to form an Integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The primary function of the auxiliary control module is to serve as the interface between the system controls such as contrast, brightness and polarity controls and the system power supply, the scanner, and the post amplifier/control driver modules. The auxiliary control module provides control and processing circuitry for gain commands, brightness and video gate commands, polarity commands and positive and negative voltage regulators.

1.3 TECHNICAL SPECIFICATIONS

The technical specifications of the Auxiliary Control module are as follows:

Parameter	Specification
IR Level and Gate out Signal	IR Level: 0 to -1.5 Vdc Gate out: +1.0 Vdc squarewave

Parameter	Specification
IR Gain Command Voltages	
Gain Command 1	-3.0 to +3.0 Vdc (nominal)*
Gain Command 2	0.0 to 0.5 Vdc (nominal)* *Voltage limits will depend on system requirements
IR Polarity Control	+0.6 ±0.25 Vdc or -3.5 ±1.5 Vdc inverted with respect to each other
Polarity Transient Protection	+1 volt (nominal) gated level on the IR level and gate waveform, duration of 140 ±40 milliseconds at each operation of polarity switch
Scan Failure Protection	Continous +1 volt (nominal) gated level on IR level and waveform when gate signal not received for duration of greater than 120 +40 milliseconds
Supply Voltage and Current	
Voltage (High Power)	+10 volts dc and -7.5 volts dc
(Low Power)	±4.8 volts dc and ±7 volts dc
Current (10 volts dc)	28 ±3 mA plus 2.5 ±1 mA/Channel
(-7.5 volts dc)	21 ±3 mA plus 2.5 ±1 mA/Channel
Regulator Outputs	
Positive	+3.0 to +4.5 Vdc (adjustable)
Negative	-3.0 to -4.5 Vdc (adjustable)

NOTE:

In mechanical specifications involved with interface requirements such as mechanical configuration, interconnection and mounting information, refer to Section III.

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The auxiliary control module serves as the interface between system controls and the system power supply, Scanner, and Post Amplifier/Control Driver modules. The module provides processing circuitry for gain control, IR level and gate control, polarity control and positive and negative voltage regulators. Test points are provided for the two gain commands, the polarity commands and the composite brightness (IR level) and video gate signal.

To develop the gain control signals, an external gain control potentiometer is connected to the input of a unity gain buffer stage which in turn drives a network of four trim potentiometers on the module. These trim controls are used to set the upper and lower limits of gain command voltages 1 and 2. The gain commands are each processed through a summing amplifier which includes a temperature compensating diode to help maintain gain stability over temperature extremes. Gain command voltages 1 and 2 are then weighted for system requirements and fed to the first and second stages of the Post Amplifier/Control Driver module as Gain Command 1 and Gain Command 2.

To develop the IR level and gate out signals, the DC voltage on the arm of an external brightness control potentiometer is similarly buffered and summed with the video gate signal. Trim potentiometers are provided to set brightness and blanking range. The polarity control signal is also fed into the brightness channel to automatically adjust display brightness when the polarity switch is activated. The polarity command and inverse polarity command are essentially the amplified and inverted signals from the polarity control switch. The circuit automatically suppresses switching transients that might occur during switching.

The positive and negative regulator circuits are both standard series pass type regulators which regulate high or low power voltage inputs from the system power supply before they are fed to the other modules of the system.

2.2 THEORY OF OPERATION

2.2.1 GAIN CONTROL CIRCUIT

The infrared gain control or gain command circuit generates and applies two gain command signals (Gain Command 1 and Gain Command 2) to externally connected video circuits. Referring to Figure 2-1, Sheet 2, the circuit consists of three integrated circuits (IC's) AR1, AR2 and AR3 and transistors Q14 and Q15.

The dc level (0 to 3 volts dc) on the wiper of an external IR Gain potentiometer is applied to the inverting input of a high impedance unity gain buffer amplifier AR1. The stable dc signal level output of AR1 is applied across trim potentiometers R37 and R38 which are adjusted to set the maximum gain of Gain Command 1 and Gain Command 2 respectively. Trim potentiometers R39 and R48 are similarly adjusted to set the minimum gain of the two gain commands. The dc levels on the wipers of R37, R48 and R38, R39 are applied to the inverting input of amplifier AR3 and AR2 respectively. Diode CR11 and associated resistors R49 and R51 provide temperature compensation to help maintain gain stability over temperature extremes.

The output of AR3 is applied to the base of drive transistor Q15 which emitter couples the dc level to connector pin P1-22 as Gain Command 1 Out signal. Similarly, the output of AR2 is applied to the base of drive transistor Q14 and emitter coupled to connector pin P1-7 as Gain Command 2 out.

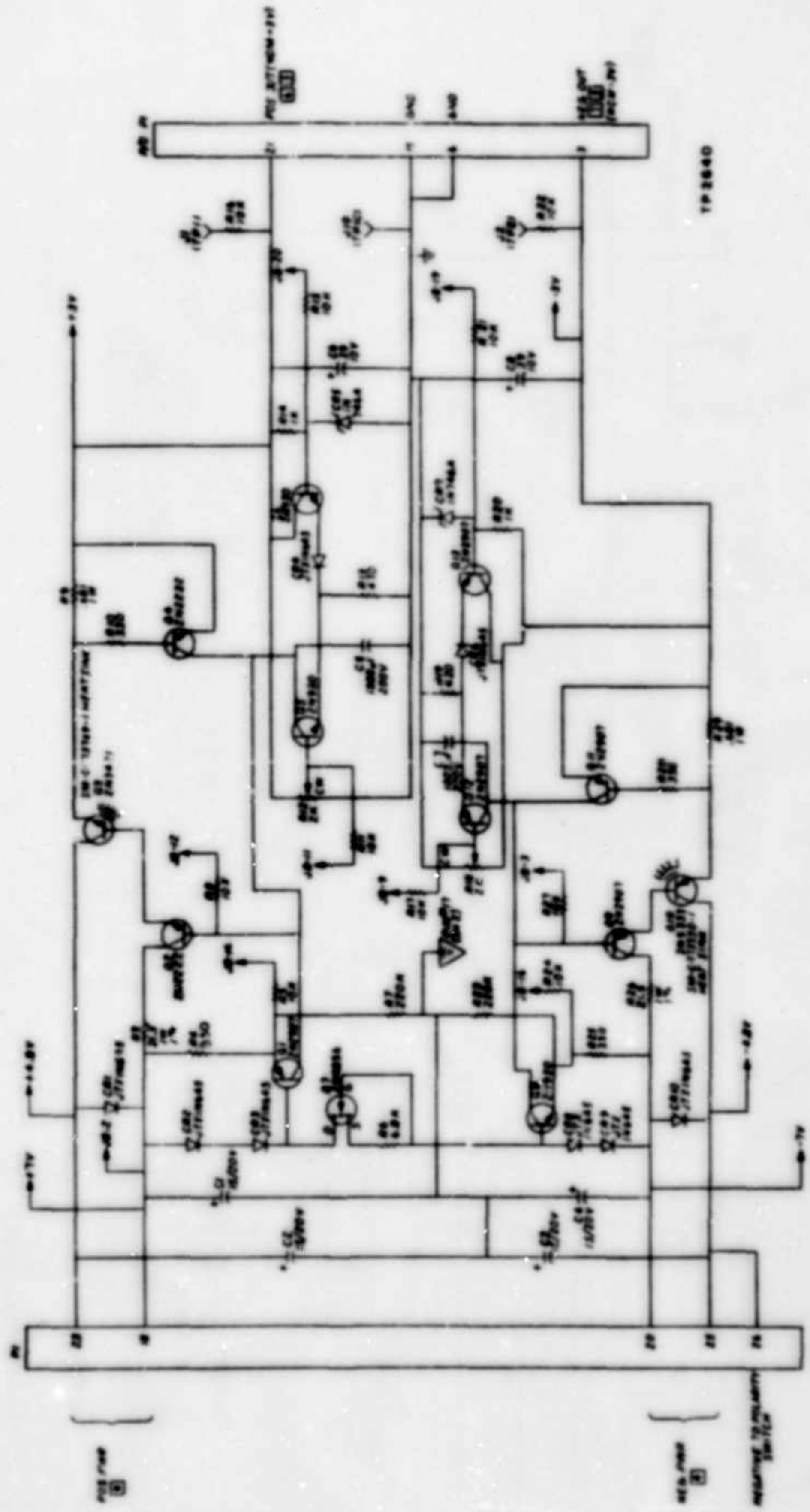


Figure 2-1. Auxiliary Control Module Schematic Diagram (Sheet 1 of 2)

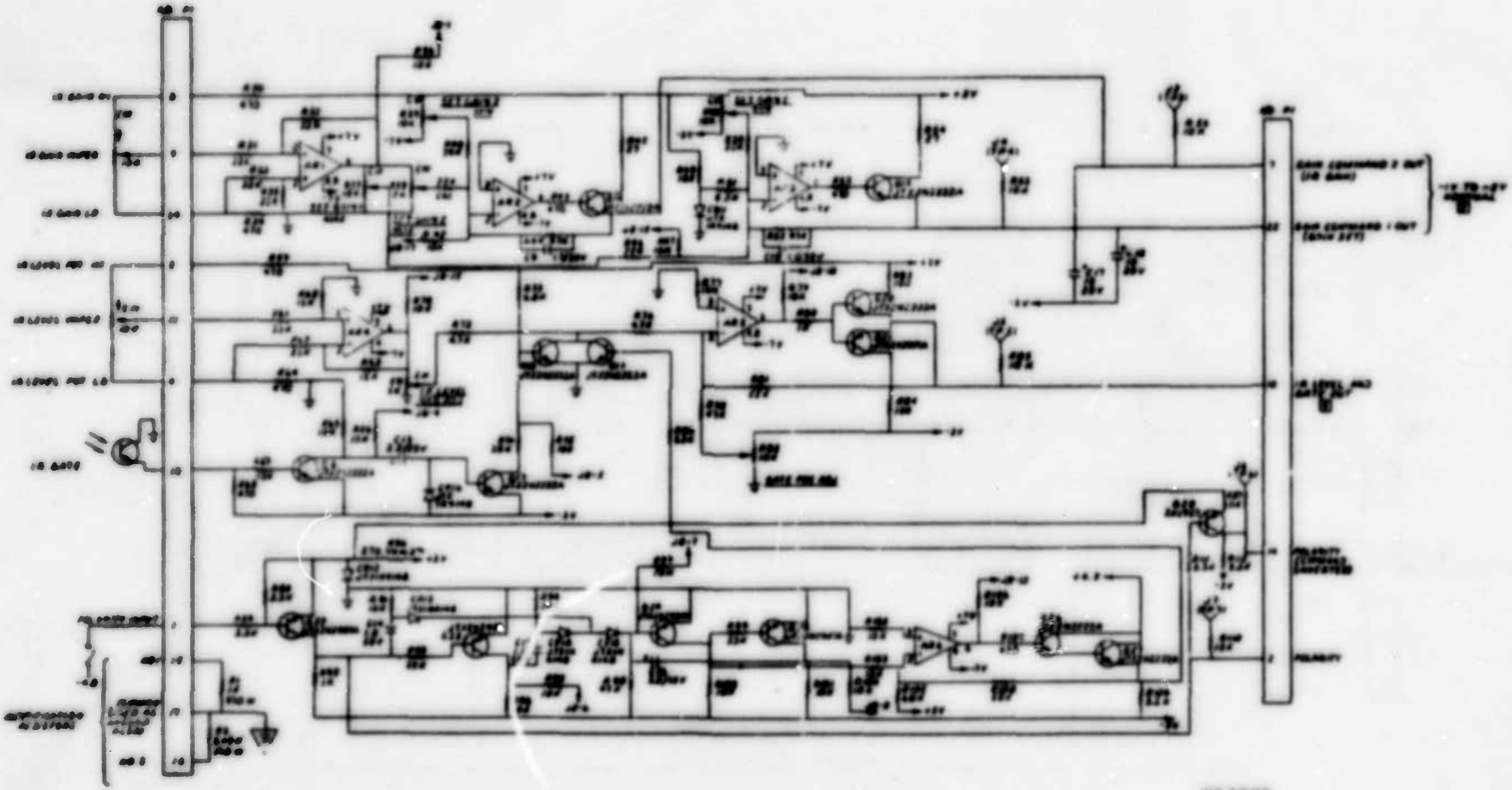


Figure 2-4. Auxiliary Control Module Schematic Diagram (Sheet 2 of 2)

The Gain Command 1 and Gain Command 2 signals are fed to the first and second stages respectively of the Post Amplifier/Control Driver module.

2.2.2 IR LEVEL AND GATE OUT SIGNAL CIRCUIT

The IR level and gate out signal circuit generates the output signal functions which control the system video signal on and off times. Referring to Figure 2-1, Sheet 2, the circuit consists of two IC amplifiers, AR4 and AR5, and six transistors, Q16 through Q21.

The dc level on the wiper of an external system brightness (IR Level) control is applied to the noninverting input of buffer amplifier AR4. The dc level output signal of AR4 is applied across potentiometer R71 (IR LEVEL NEG. ADJ.) which is used to set the system brightness range. Potentiometer R82 (GATE POS ADJ) is used to set the system blanking range. The wipers of R71 and R82 are applied to the inverting input of amplifier AR5. The IR gate pulse and polarity transient suppression signals are also added to the IR level at this point as described in more detail in following paragraphs. The output of AR5 is applied to the bases of complementary coupled drive transistors Q20 and Q21 and is emitter coupled by Q20 and Q21 to the externally connected video circuits through connector pin PI-10 as the IR Level and Gate Out signal.

The IR Gate pulse generated during scan turn around by the Scan & Interlace module is applied to the base of transistor Q16, turning Q16 on. The output pulse of Q16 is capacitively coupled by capacitor C13 to the base of transistor Q17 turning Q17 off. Will Q17 off, the base of transistor Q18 is biased on for the duration of the IR Gate pulse input. With Q18 on, the IR Gate pulse is added to the IR level at the inverting input of amplifier AR5. The design of the IR Gate circuit also provides scan failure protection. Failure of

an IR Gate pulse input for a period greater than 120 ±40 milliseconds permits capacitor C13 to charge to its peak value through the emitter base junction of transistor Q17. When C13 approaches its peak charge, the base of Q17 will be reverse biased shutting Q17 off. With Q17 off, transistor Q18 is turned on and holds the IR level and gate out signal in the gate mode. This protects an image intensifier tube or other pick-up device such as a vidicon tube from damage that might occur if allowed to dwell on an emitter array without scan for an extended period of time.

2.2.3 POLARITY CONTROL CIRCUIT

The polarity control circuit generates the polarity and inverted polarity commands for the system video circuits and a polarity transient suppression signal which is added to the IR Level and Gate Out signal to prevent blooming of the viewed video display when the polarity switch is activated. Referring to Figure 2-1, Sheet 2, the circuit consists of transistors Q22 through Q28 and IC amplifier AR6.

Activating the external system polarity switch connected to connector pin P1-1 applies -4.8 volts dc to the base of buffer amplifier transistor Q22, turning Q22 on. The signal on the collector of Q22 is sent to the video system through connector pin P1-2 as Polarity Command. In addition the signal is also inverted by transistor Q28 and sent to the video system through connector pin P1-14 as Polarity Command (Inverted).

When buffer amplifier Q22 is turned on by activation of the polarity switch, the voltage drop across resistor R92 turns pulse shaper transistor Q23 off developing a negative going pulse on the collector of transistor Q24. The negative going pulse is capacitive coupled by capacitor C15 and forward biases diodes CR14 and CR15 thus turning Q24 off. With Q24 off,

transistor Q25 is turned on and discharges capacitor C16. The resultant square wave shaped output pulse from the collector of Schmitt-trigger circuit transistor Q24 is applied to the inverting input of IC amplifier AR6. The output of AR6 is applied to driver transistors Q26 and Q27. The output from the emitter of Q27 is applied to the base of transistor Q19. Thus, the polarity transient suppression signal on the collector of Q19 is added to the IR Level at the inverting input of AR5 to prevent blooming on the viewed video display when the system polarity switch is activated.

2.2.4 VOLTAGE REGULATOR CIRCUITS

The positive and negative voltage regulator circuits are both standard series pass regulators. They are designed to operate in either of two modes; a low power mode (±4.8 volts dc and ±7 volts dc), or a high power mode (+10 volts dc and -7.5 volts dc). Referring to Figure 2-1, Sheet 1, the positive voltage regulator consists of transistors Q1 through Q6 and the negative voltage regulator transistors Q8 through Q13 with FET transistor Q7 common to both regulators. Since the positive and negative voltage regulators are mirror images of each other and both operate in the same manner, the description of the positive voltage regulator provided in following paragraphs will also hold true for the negative regulator with appropriate changes in reference designations.

In the high power mode, the +10 volts dc supply voltage from the system power supply is applied to the collector of series pass transistor Q3 through connector pin P1-23. The base current of Q3, and therefore the voltage drop across Q3 and the resultant output voltage at the emitter, is controlled by drive transistor Q2. FET transistor Q7 acts like a variable resistor to

keep the voltage across diodes CR2 and CR3 constant, thus maintaining the base-emitter voltage of transistor Q1 constant. Therefore, transistor Q1 acts as a constant current source to provide current drive to transistors Q2, Q3 and Q4.

In the low power mode, operation is similar to that described above except that transistor Q2 acts as the series pass transistor instead of Q3. The low power supply voltage is applied to the collector of Q2 through connector pin P1-18. Transistor Q3 acts like a diode because, with reverse bias on diode CR1, the collector of Q3 is an open circuit.

Transistors Q5 and Q6 form a voltage sensing differential amplifier which compares the portion of the output voltage established by the setting of potentiometer R12 and applied by the wiper to the base of Q5 to a reference voltage on the base of Q6 established by resistor R14 and zener diode CR5. Should the output voltage start to increase, the base drive of Q5 increases, decreasing the drive current to transistors Q2 and Q3, and returning the output voltage to the value established by the setting of R12. Should the output voltage start to decrease the base drive of Q5 decreases, thus increasing the current through Q2 and Q3 until the output voltage returns to normal. Potentiometer R12 providing the voltage sensing voltage to the base of Q5 can be adjusted to provide a regulated output voltage of from +3.0 to 4.5 volts dc.

Transistor Q4 acts as a current limiter to provide short circuit over current protection. Under normal operating conditions, the voltage drop across resistor R9 is not sufficient to bias Q4 on. However, if a short circuit condition should develop in the externally connected load, the voltage drop across R9 would increase sufficiently to turn Q4 on. With Q4 on, the base

drive current supplied to Q2 by the constant current source would be used by Q4 thus decreasing the current available for Q2 and Q3. Turning off Q2 and Q3 protects the module from damage due to excessive current over loads.

SECTION III

INTERFACE

3.1 CONFIGURATION

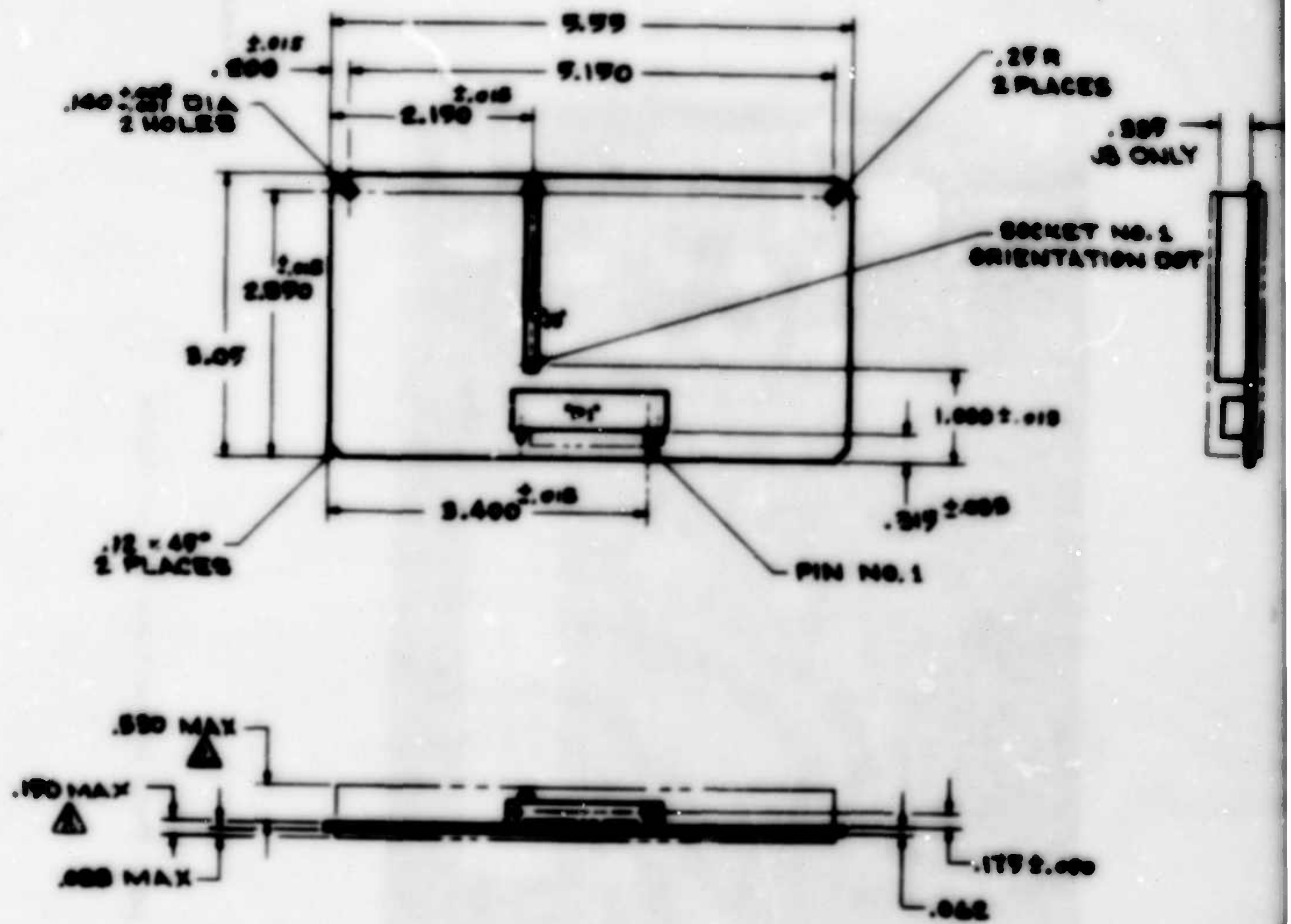
Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating the Auxiliary Control module in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is a photograph of the module and Figure 3-3 is a parts location drawing.

3.2 INTERCONNECTING INFORMATION

All signals and commands are connected through P1 to a connector on a motherboard or wiring harness. The test connector J8 is not used in normal operation but the designer should consider providing clearance so that a test plug can be connected to it without need for using an extender for P1. Access should be provided to the trim potentiometers at the top of the module. Each end of the module must be supported by a suitable mounting slide. For applications involving severe shock or vibration, positive means should be provided to retain the module in the fully engaged position.

3.3 THERMAL DESIGN CONSIDERATIONS

Although the Auxiliary Control Module power dissipation is only 2.24 watts, relatively small in the overall system, it must be taken into account during system design. Refer to Section III of Chapter 1 for a detailed discussion of the system thermal design considerations.



Tolerances:

.xx = ±.02

.xxx = ±.010

NOTES:

[illegible] SPEC DENOTES THIS DIM. AS .11 MAX.

[illegible] SPEC DENOTES THIS DIM. AS [illegible] MAX.

Figure 3-1 Auxiliary Control Module Outline Drawing

Figure 3-2 Photo of Auxiliary Control Module

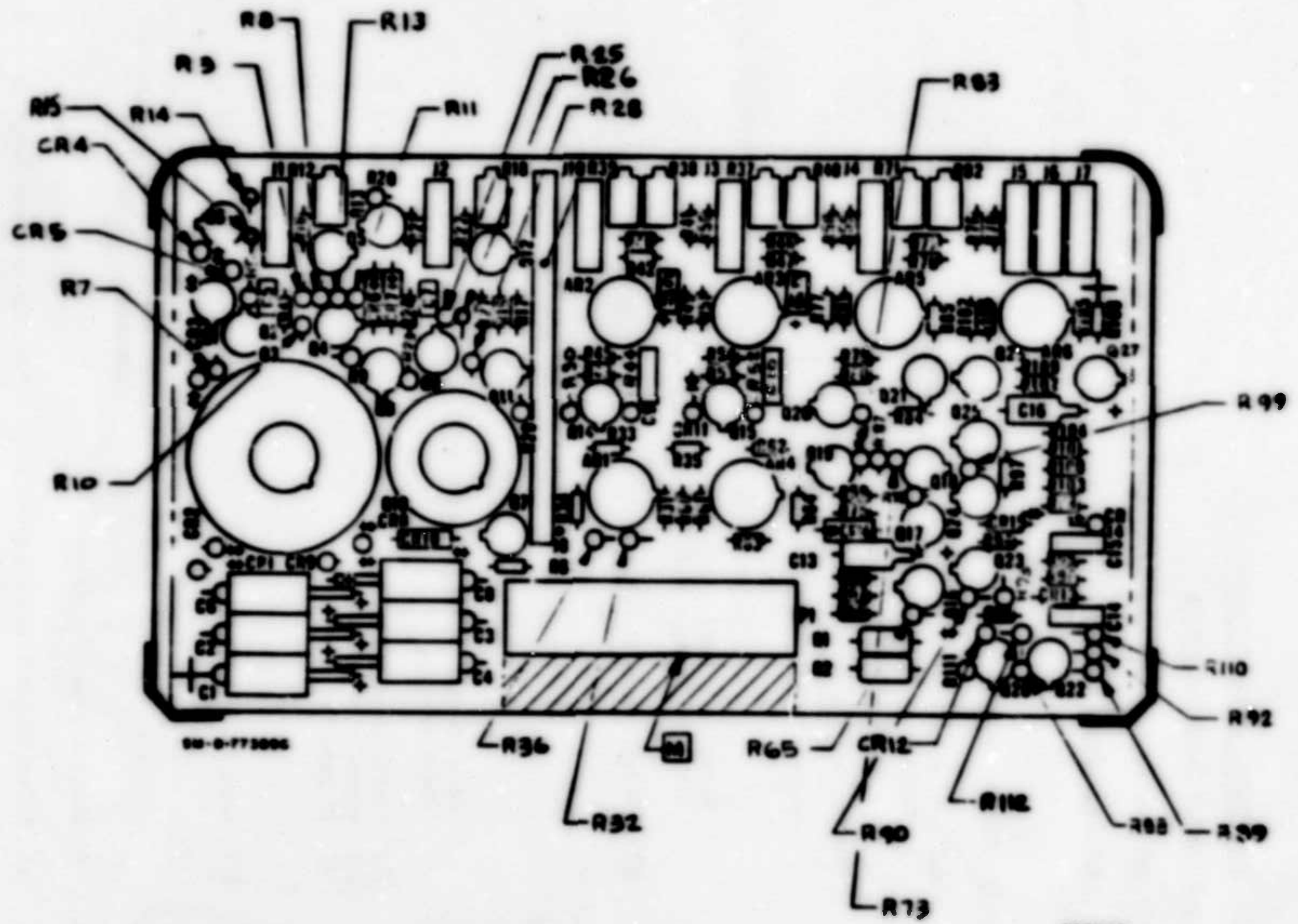


Figure 3-3. Auxiliary Control Module-Parts Location Drawing
Drawing No. SM-D-773096

Sheet 1 of 2

3.4 ELECTRICAL INTERFACE DATA

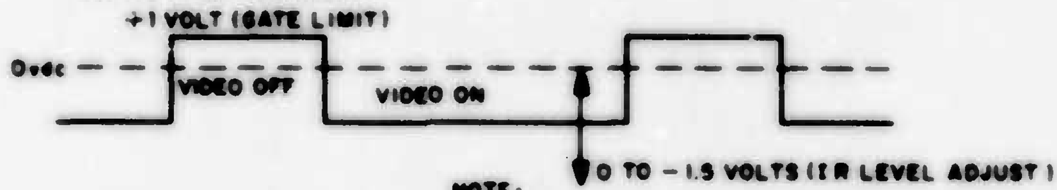
3.4.1 INPUT CHARACTERISTICS

(a) Voltage: +10 and -7.5 volts dc or + 4.8, and +7, -7 volts dc

(b) Current: 28 ±3 milliamperes plus 2.5 ±1 milliamperes per channel at +10 volts dc and 21 ±3 milliamperes plus 2.5 ±1 milliamperes per channel at -7.5 volts dc

3.4.2 OUTPUT CHARACTERISTICS

(a) IR level and gate: rectangular waveform, +1 and 0 to -1.5 volts nominal as follows:



NOTE:

Repetition rate, duty cycle, and waveform voltage limits will depend on system requirements.

(b) IR gain command voltages: gain command voltage 1, -3.0 to +3.0 volts dc nominal; gain command voltage 2, 0 to 0.5 volt dc nominal

NOTE:

Gain command voltage limits will depend on system requirements.

(c) Positive regulator: adjustable, +3.0 to +4.5 volts dc

(d) Negative regulator: adjustable, -3.0 to -4.5 volts dc

(e) IR polarity control: +0.6 ±0.25 volt dc or -3.5 ±1.5 volts dc; outputs will be inverted with respect to each other

(f) Scan failure protect: continuous gated level of +1 volt nominal on IR level and gate waveform when gate signal not received for duration greater than 120 ±40 milliseconds

3.4.3 PROCESSING CHARACTERISTICS

(a) Polarity transient suppression: Provides a gated level of +1 volt nominal on IR level and gate waveform for 140 ±40 milliseconds at each operation of system polarity switch

3.4.4 ANCILLARY ELECTRICAL DESIGN CONSIDERATIONS

(1) Although the Auxiliary Control module has a specified regulated adjustable output of from +3.0 to +4.5 volts dc, it should be noted that zener diode N746A (CR5 on schematic diagram Figure 2-1, sheet 1), used in the regulator circuit, has a rating of 3.3 volts. If a voltage ranging from +3.0 to 3.3 volts is attempted to be used, excessive ripple and a non-regulated output is likely to be obtained.

(2) The Auxiliary Control module is capable of operating with a "low power system supply voltage" or a "high power system supply voltage" as follows:

Connector P1 (pin No.)*	Low Power System Supply Voltage (volts, dc)	High Power System Supply Voltage (volts, dc)
18	+7.0	No connection
23	+4.8	+10.0
20	-7.0	- 7.5
25	-4.8	- 7.5

*See schematic diagram Figure 2-1, sheet 1

There is no advantage in operating the Auxiliary Control with the "high power" supply voltages. If the system unique power supply has the capability of supplying the "low power" supply voltages, the "low power" supply voltages should be used.

(3) The Postamplifier voltage gain is programmable from 10,000 to 18,000 volts per volt by means of the "Gain Command" outputs of the Auxiliary Control module. The "Gain Command" outputs are set by 10,000 ohm resistors R37, R38, R39 and R48 (see schematic diagram Figure 2-1, Sheet 2) and must be adjusted to provide the gain as required by the system.

(4) The IR Gain (Contrast), IR Level (Brightness) and Polarity control shown on schematic diagram Figure 2-1, Sheet 2 are part of the system unique Front Panel and are shown for reference only.

(5) The system required IR Level and Video ON-OFF time are provided by adjustments of resistors R71, 5000 ohms and R82, 10,000 ohms repectively (see schematic diagram Figure 2-1, Sheet 2) and must be set appropriately.

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the Auxiliary Control Module.

Presented herein are the test equipment requirements, test set up, adjustment, and alignment techniques.

4.2 TEST EQUIPMENT

The following, or equivalent, test equipment is required to perform the necessary operational tests, alignments, adjustments on the Auxiliary Control Module.

4.2.1 STANDARD TEST EQUIPMENT

Table 4-1, following, presents a listing of commercially available equipment which has been found to be adequate for testing of this module.

TABLE 4-1

STANDARD TEST EQUIPMENT

EQUIPMENT	MANUFACTURER	MODULE
Power Supply	Lambda	LPD422 FM
Oscilloscope	Tektronics	453
Function Generator	Wavetek	110
Digital Multimeter	Fluke	8000A

4.2.2 SPECIAL TEST EQUIPMENT

A test set should be fabricated to provide a convenient means of mounting the module, interconnecting test equipment, and providing the input control and load simulation required. See Figure 4-1.

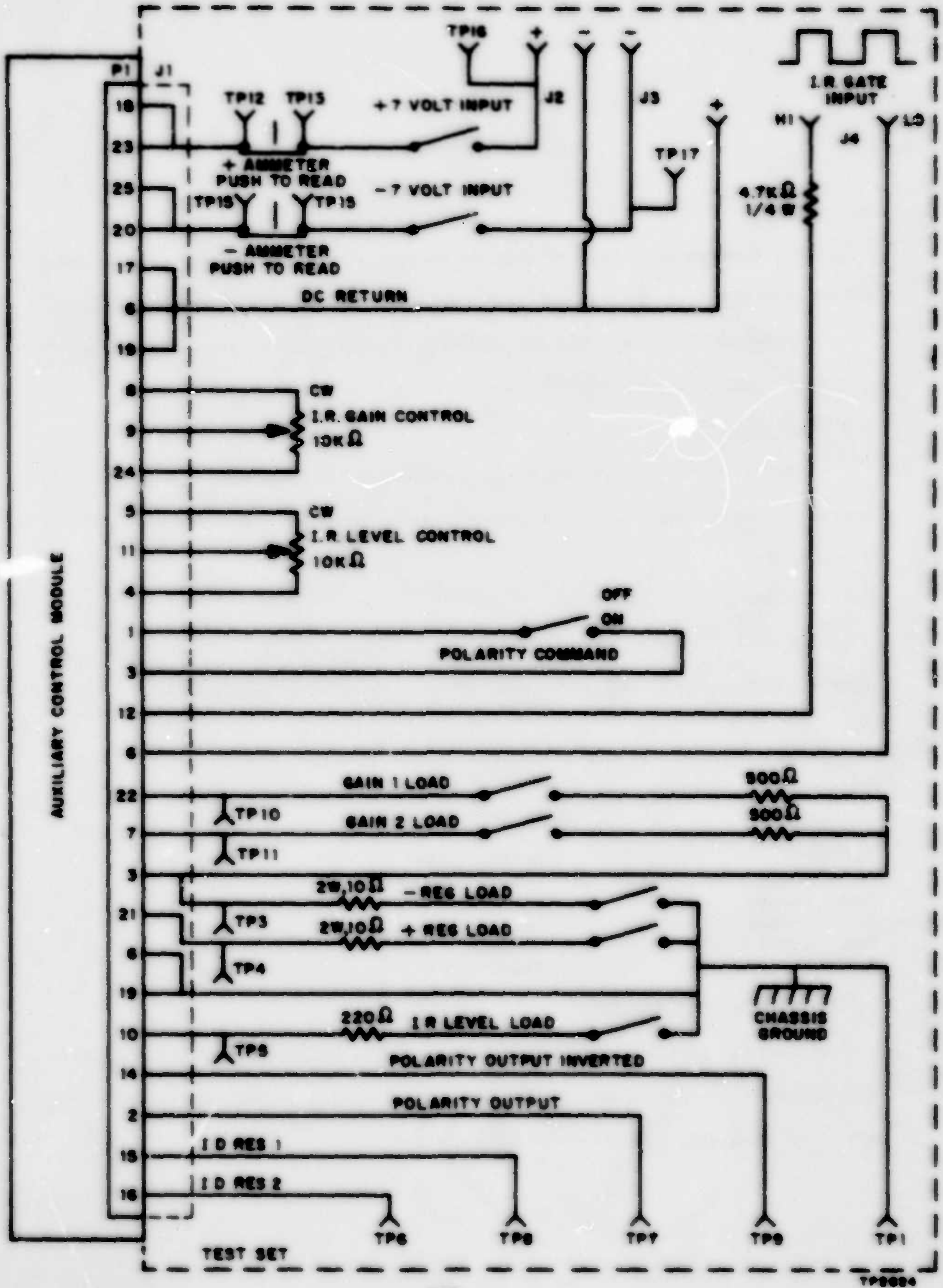


Figure 4-1 Auxiliary Control Module Test Set

4.3 SPECIAL TOOLS

No special tools are required to test the Auxiliary Control Module.

4.4 TEST SET UP

A typical test set up inter-connection diagram is shown in Figure 4-2

4.5 CALIBRATION-PREPARATION FOR USE

Operational status of the Auxiliary Control Module may be determined by the following tests.

4.5.1 ELECTRICAL TESTS AND ADJUSTMENTS

Perform each test in the order presented. As each action is completed, verify a proper response before proceeding to the next.

4.5.1.1 Equipment Interconnection

4.5.1.1.1 Connect the Auxiliary Control Module to the test set as shown in Figure 4-1.

4.5.1.1.2 Using the ohmmeter function of the digital multimeter, measure the resistance between test point 8 and test point 1.

The resistance shall be 1.0 K ohm ±0.02 K ohm.

4.5.1.1.3 Measure the resistance between test point 1 and test point 6.

The resistance shall be 5.49K ohm ±0.11K ohm.

4.5.1.1.4 Interconnect the test set and test equipment as shown in Figure 4-2.

4.5.1.1.5 Verify that all the above interconnections are properly made.

4.5.1.1.6 Turn all test equipment on and adjust the power supplies to +7.0V ±0.1 and -7.0 ±0.1V.

4.5.1.2 Input Current Measurement

Using the milliammeter function of the digital multimeter measure the current being drawn from each of the supplies by the Auxiliary Control Module.

The current shall be 18.0 ma ±5 ma for each of the supplies

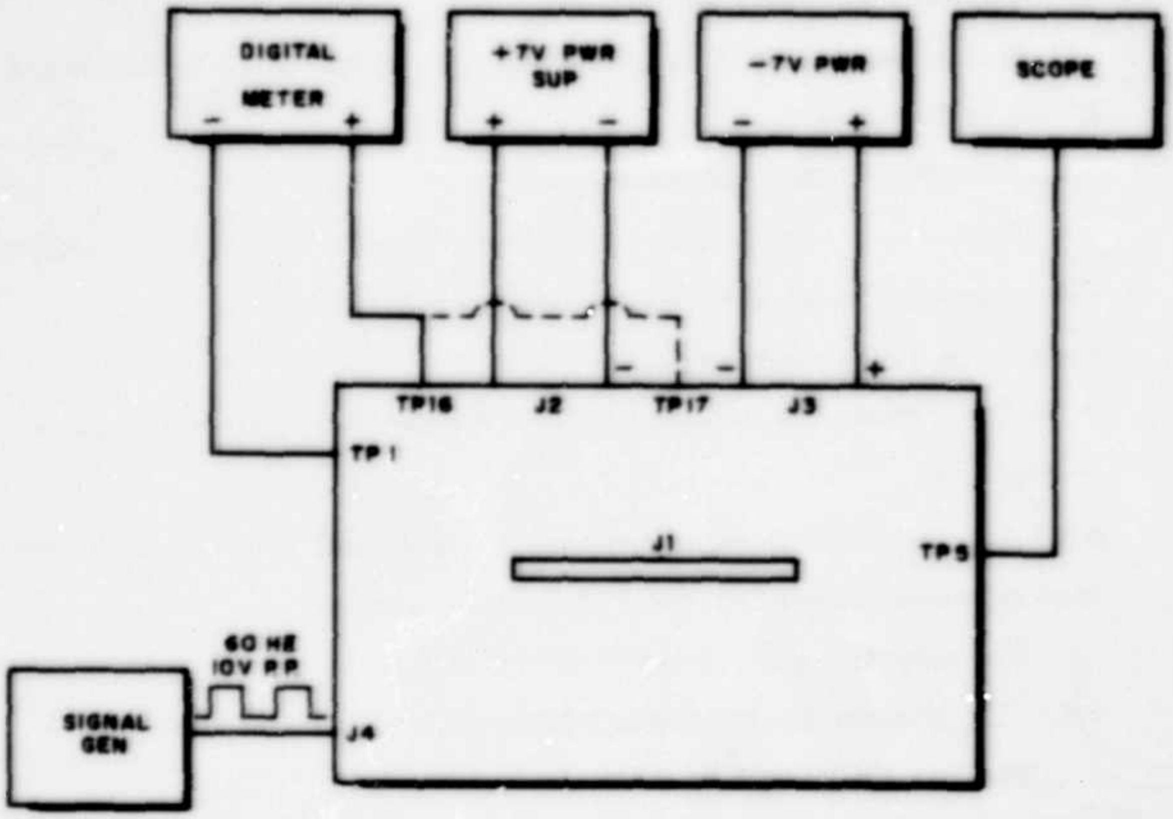


Figure 4-2 Auxiliary Control Module Test Setup

4.5.1.3 Positive Regulator Output Range/Regulation

4.5.1.3.1 With the digital multimeter, in voltage mode, connected to test point 4, adjust the positive regulator potentiometer, R12 on the module, over its full range. (see Figure 4-3 for location of R12).

The output voltage shall vary between +3.0 to 4.5 Vdc.

4.5.1.3.2 Readjust positive regulator potentiometer to 3.5 ±0.1V at test point 4.

4.5.1.3.3 Momentarily depress the +Reg Load switch. Note: the digital meter indication.

The difference between the readings of 4.5.1.3.2 and 4.5.1.3.3 shall be no more than 30 millivolts.

4.5.1.4 Negative Regulator Output Range/Regulation

4.5.1.4.1 Connect the digital meter to test point 3 and adjust the negative regulator potentiometer, R18 on the module, over its full range. (see Figure 4-3)

The output voltage shall vary between -3.0 to -4.5 Vdc.

4.5.1.4.2 Readjust the Negative Regulator potentiometer to -3.5 ±0.1V at test point 3.

4.5.1.4.3 Momentarily depress the - Reg Load switch. Note the reading,

The difference between the readings of 4.5.1.4.2 and 4.5.1.4.3 shall be no more than 30 millivolts.

4.5.1.5 Gain Command Range/Regulation

4.5.1.5.1 Adjust the test set IR Gain Control to maximum clockwise position.

4.5.1.5.2 Adjust module Gain Command 1 and 2 Max Adj (R37 and R38) to full counter clockwise position.

4.5.1.5.3 Connect the digital meter to test point 11. Adjust module Gain Command 2 Min Adj (R39) to obtain -2.0 ±0.1 Vdc at test point 11

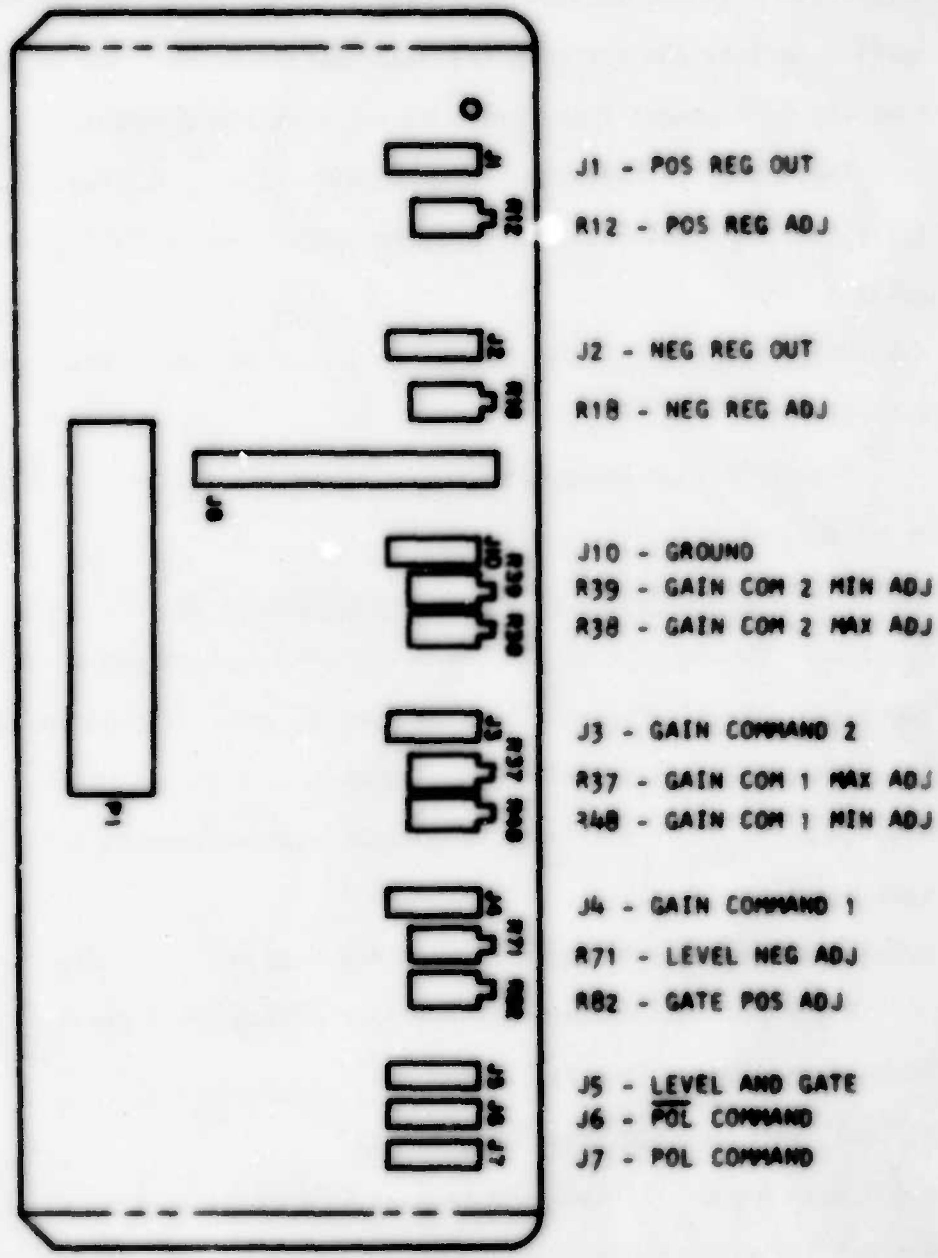


Figure 4-3. Auxiliary Control Location Of Potentiometers, Test Points, and Connectors

4.5.1.5.4 Connect the digital meter to test point 10. Adjust module Gain Command 1 Min Adj (R48) to obtain -2.0 ±0.1 Vdc at test point 10.

4.5.1.5.5 Adjust module Gain Command 1 Max Adj (R37) to obtain 1.0 ±0.1Vdc at test point 10.

4.5.1.5.6 Connect the digital meter to test point 11. Adjust module Gain Command 2 Max Adj (R38) to obtain + 2.0 ±0.1 Vdc at test point 11.

4.5.1.5.7 Rotate the test set IR Gain Control over its full range.

The Gain 2 output voltage at test point 11 shall vary between +2.0 ±0.1 Vdc to -2.0 ±0.1 Vdc.

4.5.1.5.8 Turn test set Gain 2 Load Switch on and repeat paragraph 4.5.1.5.7.

The gain 2 output voltage shall vary between +2.0 ±0.1 Vdc to -2.0 ±0.1 Vdc.

4.5.1.5.9 Move the meter connection to test point 10 to monitor the range for gain 1.

4.5.1.5.10 Adjust the test set IR Gain Control over its full range.

The Gain 1 output voltage at test point 10 shall vary between +1.0 ±0.1 Vdc to -2.0 ±0.1 Vdc.

4.5.1.5.11 Turn test set Gain 1 Load switch on and repeat paragraph 4.5.1.5.10

4.5.1.6 <u>IR Level Command Range/Regulation</u>

4.5.1.6.1 Set the Test set IR Level Control to its full clockwise position.

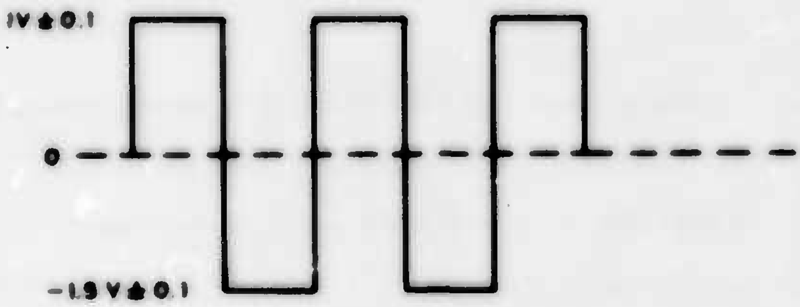
4.5.1.6.2 Set the module IR Level Neg Adj (R71) fully counter clockwise.

4.5.1.6.3 Apply a 10 volt, 60 Hz signal to the test set IR Gate input as shown in Figure 4-2.

4.5.1.6.4 Monitor the IR Level output with an oscilloscope connected to testpoint 5.

4.5.1.6.5 Adjust module Gate Pos Adj (R82) to set the positive portion of the waveform to 1.0 ±0.1 volts. (See Figure 4-4)

4.5.1.6.6 Adjust module Level Neg Adj (R71) to set the negative portion of the waveform to -1.5 ±0.1 volts. (see Figure 4-4)

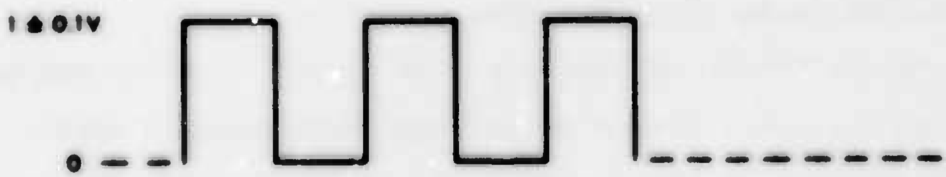


IR GATE LEVEL OUTPUT (IR LEVEL CONTROL MAX CW)

FIGURE 4-4

4.5.1.6.7 Rotate the test set IR Level Control from its fully clockwise position to fully counter clockwise and back to fully clockwise.

The output voltage shall vary from that shown in Figure 4-4 to that of Figure 4-5, and return to Figure 4-4.



IR GATE LEVEL OUTPUT (IR LEVEL CONTROL MAX CCW)

FIGURE 4-5

4.5.1.6.8 Turn test set IR Level Load switch on and repeat paragraph 4.5.1.6.6

4.5.1.7 Polarity Command Output (Switch Off)

4.5.1.7.1 Measure the voltage output at test set test point 9.

The voltage shall be 0.6 ±.25 Vdc.

4.5.1.7.2 Measure the voltage output at test set test point 7.

The voltage shall be -3.5 ±1.5 Vdc.

4.5.1.8 Polarity Command Output (Switch On)

4.5.1.8.1 Measure the voltage output at test set test point 9.

The voltage shall be -3.5 ±1.5 Vdc.

4.5.1.8.2 Measure the voltage at test set test point 7.

The voltage shall be 0.6 ±.25 Vdc.

4.5.2 MECHANICAL ALIGNMENT

No mechanical alignment is required for the Auxiliary Control Module, however, system layout should provide for convenient accessibility to the eight adjustment potentiometers.

4.5.3 ADJUSTMENT IN THE SYSTEM

Adjustment of the Gain Command Voltages, IR Level and Gate Period, and Positive and Negative Regulated Voltages depend on the using system requirements. Accordingly, no detailed procedure is presented here.

As preliminary steps when system requirements have been established, the procedure outlined in paragraph 4.5.1 may be followed, substituting the required system levels for those presented herein.

4.6. SPECIAL MAINTENANCE REQUIREMENTS

The Auxiliary Control Module requires no special maintenance attention other than the routine procedures followed for general electronic equipment. No time change components are contained in this module.

CHAPTER 5

REGULATOR, DETECTOR BIAS, INFRARED

USAECOM SM-D-773914

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Infrared Bias Regulator module hereinafter called the bias regulator supplies a highly regulated, low noise, low impedence source of 5 volts dc power to the detector/dewar module. The bias regulator is capable of providing 6 milliamperes per channel up to a maximum of 180 channels or 1.2 amperes maximum. The bias regulator is comprised of discrete transistors, power transistor heatsinks and discrete components mounted on a printed wiring board (PWB).

1.2 INTENDED USE OF ITEM

The bias regulator module has been designed to be interfaced with other major common and special modules to form an integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The primary function of the bias regulator is to convert a +9.5 to 10 volt dc primary power input from the system power supply into a source of highly regulated, low noise, low impedance 5 volts dc at 1.2 ampere power to supply the bias voltage for the detector elements of the common or a special detector/dewar module.

1.3 TECHNICAL SPECIFICATIONS

The technical specifications for the Bias Regulator module are as follows:

Parameter	Specification
Input Voltage and Current	
Voltage	+9.5 to 10 volts dc
Current (+10 Vdc Input)	13 ±0.004 milliamperes (no load)
Output Voltage and Current	
Voltage	+5 ±0.2 volts dc at 23° ±2°C +5 ±0.5 volts dc -54° +71°C
Current	1.2 amperes or 6 milliamperes per channel up to a maximum of 180 channels
Current Limiting	1.5 ±0.25 amp
Output Impedance	0.3 ohm to 50 kHz
Line Rejection	50 dB to 50 kHz

NOTE

For mechanical specifications involved with interface requirements such as mechanical configuration, interconnection and mounting information, refer to Section III.

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The bias regulator module supplies a highly regulated, low noise, low impedence source of 5 volt dc bias voltage to the detector elements of the detector/ dewar module. The regulator circuit is a standard dissipative series pass regulator. One unique characteristic of the module is the grounding arrangement. The return from the detector common should be made directly to the source ground to eliminate noise from the return circuit. To prevent ground loops, the output return is not connected to the input return on the module. However, if the external ground connection is interrupted or missing, diode CR4 or CR5 (See Figure 2-1) will switch on to complete the return path.

2.2 THEORY OF OPERATION

2.2.1 CIRCUIT DESCRIPTION

The +9.5 to 10 volts dc from the system power supply enters the module at connector pin P1-5 and is applied to the collectors of drive transistors Q2 and Q3 and series pass transistors Q4 and Q5 (See Figure 2-1). The base current of Q4 and Q5, and therefore, the voltage drop across Q4 and Q5 and the resultant output voltage at the emitters, is controlled by drive transistors Q2 and Q3. FET transistor Q7 acts like a variable resistor to keep the voltage across diodes CR2 and CR3 constant. With the voltage across CR2 and CR3 constant, the base-emitter voltage of transistor Q1 acts as a constant current source to supply the current drive to the series pass regulator transistors Q2, Q3, Q4 and Q5.

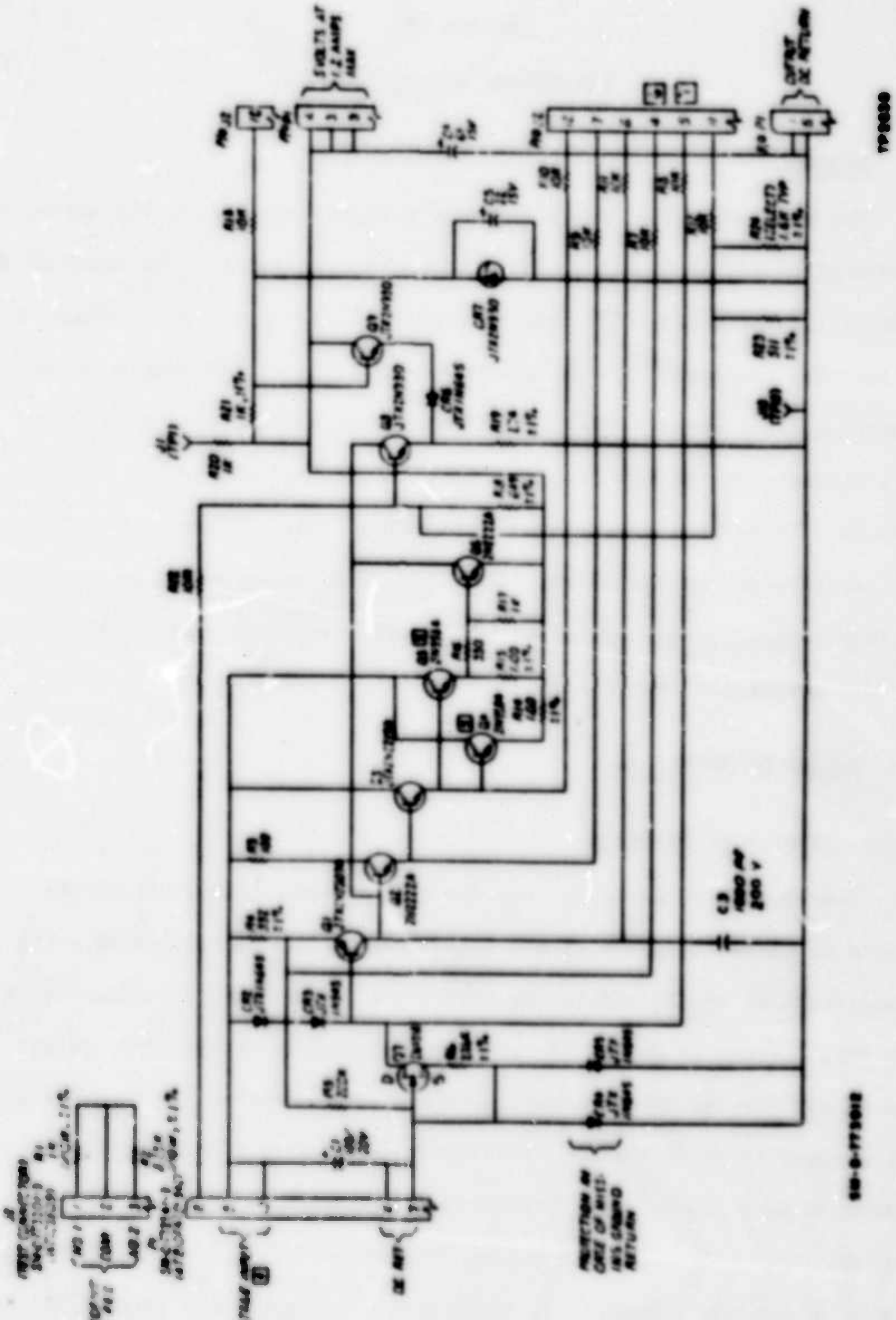


Figure 2.1. Bias Regulator Module Schematic Diagram

Transistors Q8 and Q9 form a voltage sensing differential amplifier which compares a sampling of the output voltage to a reference voltage. Resistors R18 and R23, R24 form a voltage sensing divider network which provides the output voltage sample applied to the base of Q8. Resistor R21 and zener diode CR7 establish the reference voltage applied to the base of Q9. The output voltage may be adjusted up or down by changing the value of trim resistor R24, thus, changing the output sample voltage at the base of Q8.

Transistor Q6 acts as a current limiter to provide short circuit protection to the module circuitry should an over current condition develope in the output voltage external load.

2.2.2 REGULATOR CIRCUIT OPERATION

The regulator circuit operates in the following manner to provide a regulated +5 volts dc at connecter pins P1-3, 4 and 9. If the output voltage tries to increase above +5 volts dc, the increase in voltage is sensed by resistors R18 and R23 and the voltage at the base of transistor Q8 increases causing the current flow through Q8 to increase. Since the current is supplied by a constant current source (Q1), the increased current flow through Q8 decreases the current drive available to series pass transistors Q2 through Q5. The decreased current flow through the series pass transistors reduces the output voltage until the +5 volts dc is attained.

When the +5 volt dc output voltage tries to decrease, the opposite sequence occurs. The base drive to Q8 decreases and the current drive through series pass transistors Q2 through Q5 increases until the output voltage again stabilize at the +5 volt dc level.

2.2.3 CURRENT LIMITER OPERATION

Transistor Q6 acts as a current limiter to provide short circuit or overcurrent protection. Under a short circuit condition, the output current is limited to 1.5 ± 0.25 amperes. The current limiter circuit operates as follows:

Under normal operating conditions with proper output loading, the voltage drop across current sensing resistors R14 and R15 is not sufficient to turn Q6 on. However, if a short circuit condition developes in the externally connected load, the voltage drop across R14 and R15 increases sufficiently to turn Q6 on. With Q6 on, the current drive supplied to series pass transistors Q2 through Q5 is decreased since the current for both circuits is a constant current source (Q1). With decreased current drive, Q2 through Q5 are turned off thus shutting down the regulator until the short circuit or overcurrent condition on the output is removed.

SECTION III

INTERFACE

3.1 CONFIGURATION

Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating the Bias Regulator module in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is a photograph of the module and Figure 3-3 is a parts location drawing.

3.2 INTERCONNECTING INFORMATION

The Bias Regulator normally connects with a connector on a mother board or wiring harness through which electrical connections are made to the Detector-Dewar module and to a power supply. Each end of the module must be supported by a suitable mounting slide. For applications involving severe shock or vibration, positive means should be provided to retain the module in normal operation, but the system designer should consider providing clearance for connection to it for testing without need for using an extender for P1.

3.3 THERMAL DESIGN CONSIDERATIONS

Although the Bias Regulator module power dissipation is only .03 watt / channel (up to 180 channels), very small in an overall system, it must be taken into account during system design. Refer to Section III of Chapter 1 for a detailed discussion of the system thermal design considerations.

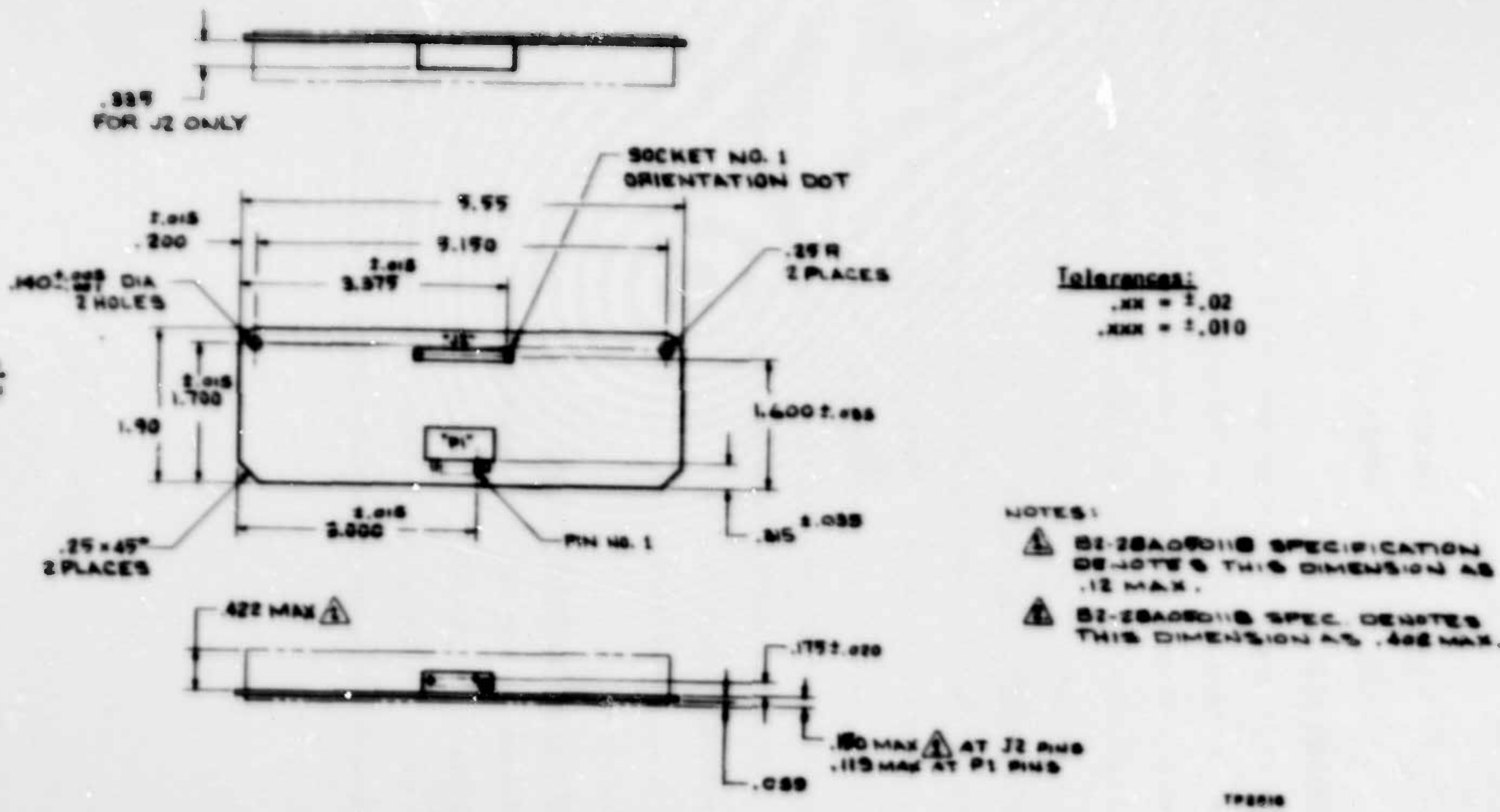
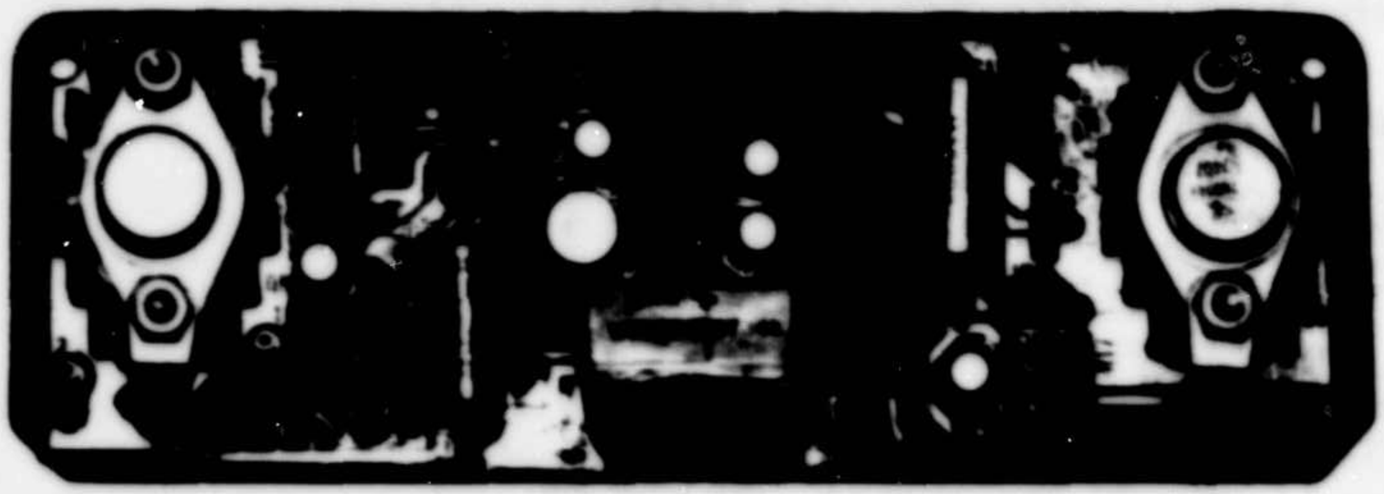


Figure 3-1 Bias Regulator Module Outline Drawing



TP2023

Figure 3-2. Photo of Bias Regulator Module

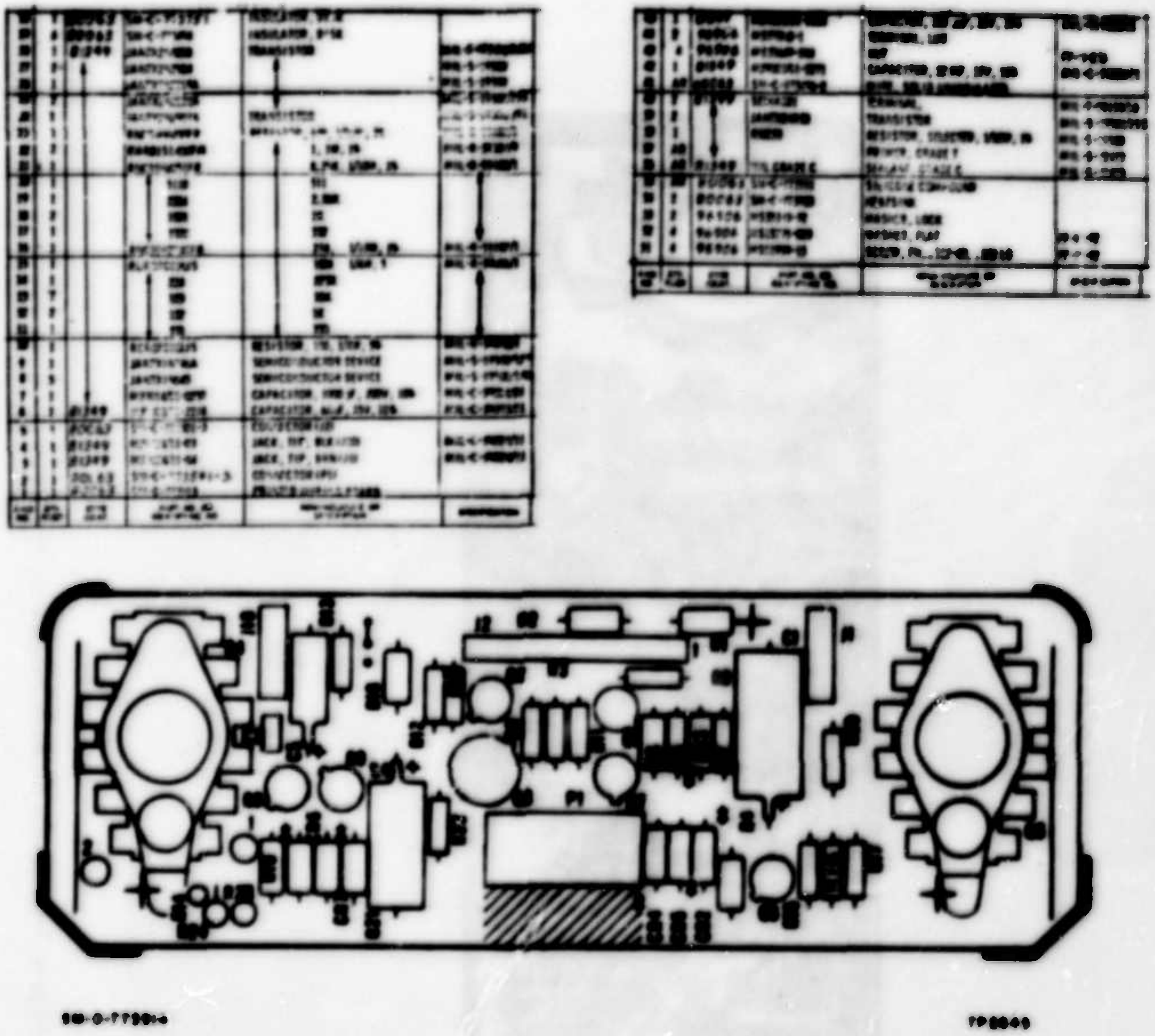


Figure 3-3. Bias Regulator Module Parts Location Drawing

3.4 ELECTRICAL INTERFACE DATA

3.3.1 INPUT CHARACTERISTICS

(a) Voltage: 9.5 to +10 volts dc

3.3.2 OUTPUT CHARACTERISTICS

(a) Current: 6 milliamperes per channel maximum for a maximum of 180 channels

(b) Voltage: +5 ±0.2 volts dc at +23 ±2°C
+5 ±0.5 volts dc from -54 to +71°C

(c) Line rejection: ratio of input peak-to-peak ripple to output peak-to-peak ripple 50dB to 50 kHz (Min)

(d) Impedance: 0.3 ohm to 50 kHz

3.3.3 PROCESSING CHARACTERISTICS

(a) Current limit: short circuit currentlilmit 1.5 ±0.25 amperes

3.3.4 ANCILLIARY ELECTRICAL DESIGN CONSIDERATIONS

(1) Since the input to the Bias Regulator Assembly can be a minimum of 9.5 volts dc and a maximum of 10.0 volts dc, and the regulated output can be a maximum of +5.5 volts dc at 1.08 amperes, the Bias Regulator Assembly can dissipate about 5 watts (substantially by heat sinked Q4 and Q5, 2N3584; see schematic drawing Figure 2-1). The Bias Regulator Assembly therefore, should not be installed adjacent to heat sensitive piece parts.

(2) The voltage input 9.5 to 10.0 volts dc) to the Bias Regulator Assembly must be supplied by a system unique power supply.

(3) If space or power are significant system design constraints, consideration should be given to using a microcircuit voltage regulator in lieu of the Bias Regulator Assembly.

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the Bias Regulator Module. Presented herein are the test equipment requirements, test set up, adjustment and alignment techniques.

4.2 TEST EQUIPMENT

The following, or equivalent, test equipment is required to perform the necessary operational tests, alignments, and adjustments on this module.

4.2.1 STANDARD TEST EQUIPMENT

Table 1, following, presents a listing of commercially available equipment which has been found to be adequate for testing of the Bias Regulator

TABLE 1

EQUIPMENT	MANUFACTURER	MODEL
Power Supply	Hewlett Packard	6291A
Digital Multimeter	Fluke	8000A

4.2.2 SPECIAL TEST EQUIPMENT

Convenient means of interconnecting the various equipment used in testing the Bias Regulator Module may be achieved by fabricating a Test Set. Such a test set may be fabricated from the information in Figure 4-1

4.3 SPECIAL TOOLS

No special tools are required to test the Bias Regulator.

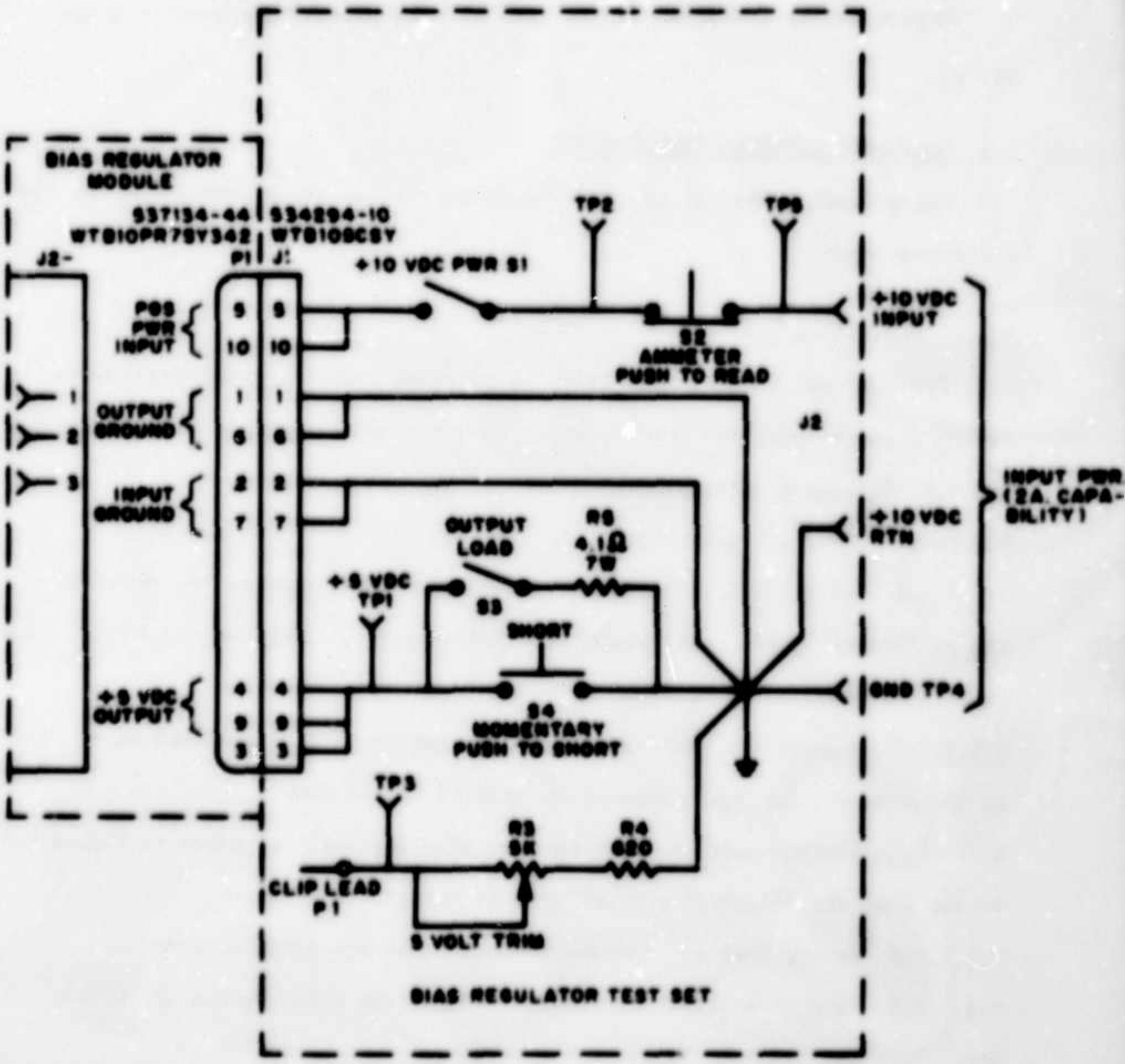


Figure 4-1 Bias Regulator Module Test Set

4.4 TEST SET UP

Figure 4-2 is a diagram of the typical interconnections used in a test set up.

4.5 CALIBRATION/PREPARATION FOR USE

Operational status of the Bias Regulator Module may be determined by the following tests.

4.5.1 ELECTRICAL TESTS AND ADJUSTMENTS

Perform each test of the following paragraphs in the order presented. Verify a proper response or indication before proceeding to subsequent actions.

4.5.1.1 Equipment Interconnection

4.5.1.1.1 Connect the module to the test set as shown in Figure 4-1.

4.5.1.1.2 Using the ohmmeter function of the digital multimeter, measure the resistance between test point J2-1 and test point J2-2 on the module. The resistance shall be 1±0.02k ohms.

4.5.1.1.3 Measure the resistance between test point J2-2 and test point J2-3 on the module. The resistance shall be 8.25 ±0.17k ohms.

4.5.1.1.4 Interconnect the test set and test equipment as shown in Figure 4-2. Insure that +10 VDC POWER and OUTPUT LOAD switch are off.

4.5.1.1.5 Verify that all the above connections are properly made.

4.5.1.1.6 Turn on all test equipment. Adjust the power supply to 10±0.1 Vdc. Turn on test set +10 VDC POWER switch.

4.5.1.2 Selection of R24

Note: This paragraph is required only if resistor R24 has not been selected and installed prior to this test. If R24 has been selected, proceed to paragraph 4.5.1.3.

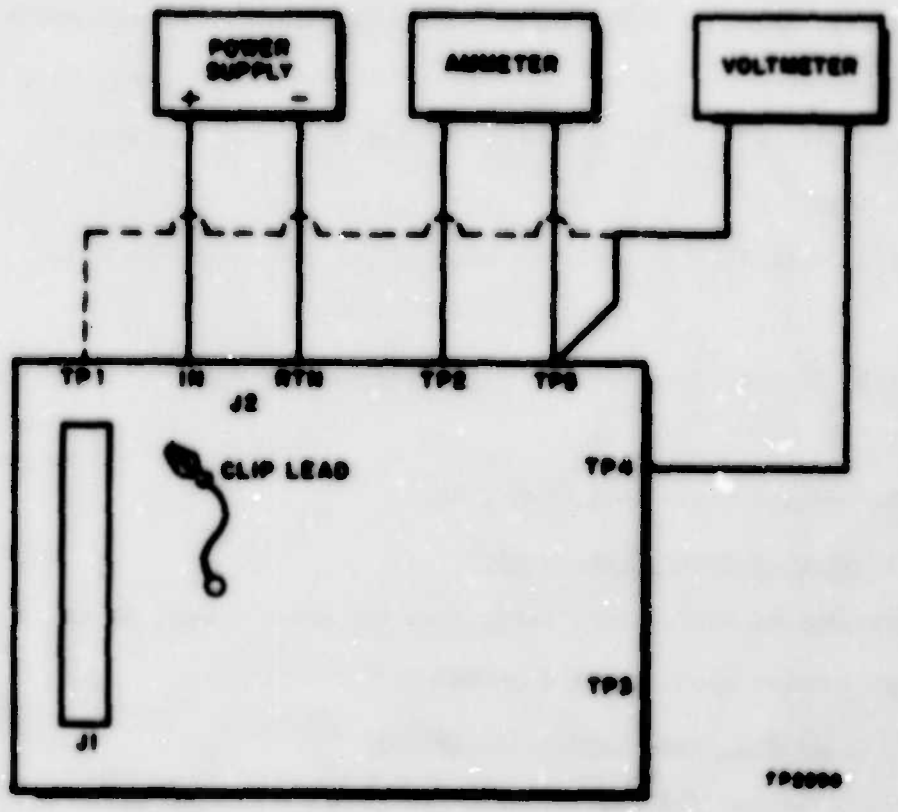


Figure 4-2 Bias Regulator Module Test Setup

4.5.1.2.1 Connect the clip lead on test set to the high side of resistor R23 on the module.

4.5.1.2.2 Adjust the test set 5 VOLT TRIM potentiometer for 5.0 ±0.2 Vdc at test point

4.5.1.2.3 Turn off test set +10 VDC POWER switch. Disconnect the clip lead from module resistor, R23. Measure the resistence from test point 3 to test point 4 to determine the correct value for circuit component R24.

4.5.1.2.4 Resistor R24 shall be installed by wiring and assembly personnel at this time.

4.5.1.2.5 With R24 installed in the module, reconnect the module to the test set.

4.5.1.2.6 Turn on test set +10 VDC POWER switch. Measure the voltage at test point 1.

The voltage shall be 5.0 ±0.2 Vdc

4.5.1.3 Input Current Measurement

Measurement the current being from the power supply by the Bias Regulator.

The current shall be 13.0 ±4.0mA

4.5.1.4 Output Voltage Output/Regulation

4.5.1.4.1 Connect the digital meter to test point 1 to measure Bias Regulator output voltage.

The voltage shall be 5.0 ±0.2 Vdc.

4.5.1.4.2 Turn on the test set OUTPUT LOAD switch. Observe output voltage reading.

The voltage shall not change more than 50 millivolts from that recorded in paragraph 4.5.1.4.1

4.5.1.4.3 With the test set OUTPUT LOAD switch on, increase theinput voltage to the module by 1.0 VDC.

The output voltage change shall be less than 20 millivolts from the reading in paragraph 4.5.1.4.2.

Turn off the OUTPUT LOAD switch.

4.5.1.5 Input Current Limit

4.5.1.5.1 Insure that the OUTPUT LOAD switch is off and that input voltage is 10.0 ±.1 Vdc.

4.5.1.5.2 Connect an ammeter to measure input current. Momentarily depress SHORT CIRCUIT switch and note current indication on the ammeter.

Short circuit current shall be 1.5 ±0.25 amps.

4.5.2 MECHANICAL ALIGNMENT

No mechanical alignment is required for the Bias Regulator Module.

4.5.3 ADJUSTMENT IN THE SYSTEM

No adjustment of the Bias Regulator is needed upon installation. Except for trim resistor R24, which is selected at test, all components are fixed value and determined at design.

4.6 SPECIAL MAINTENANCE

The Bias Regulator Module requires no special maintenance attention beyond the routine procedures followed for general electronic equipment. No time change components are contained in this module.

CHAPTER 6

DC/AC INVERTER ASSEMBLY

USAECOM SM-D-773433

PART OF

COOLER/INVERTER, INFRARED MODULE

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

1.1.1 COOLER/INVERTER, INFRARED

The Cooler/Inverter, Infrared common module is comprised of two seperately functioning assemblies; the DC/AC Inverter Assembly and the Moduler Cooler Assembly. This chapter of the manual describes the functioning and provides design information on the DC/AC Inverter. The Modular Cooler is covered in chapter 7 of the manual.

1.1.2 DC/AC INVERTER

The DC/AC Inverter converts 24 volts dc at 2.0 amperes system power into a 115 volts ac, 400 Hz, 2-phase power source for the universal motor within the externally connected Modular Cooler. The assembly can also supply 24 volts pp (12 volts rms) to power the motor of a system cooling fan if one is required.

1.2 INTENDED USE OF ITEM

The Cooler/Inverter, Infrared common module comprised of two assemblies, the DC/AC Inverter and the Modular Cooler, has been designed to be interfaced with other major common and special modules to form an Integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The DC/AC Inverter assembly has been specifically designed to supply the 115 Vac, 400 Hz, 2 phase power required to drive the universal motor in the Modular Cooler and form an Integrated Cooler/Inverter common module.

1.3 TECHNICAL SPECIFICATIONS

The technical specifications of the DC/AC Inverter Assembly are as follows:

Parameter	Specification
Input	
Voltage	24±4 volts dc
Current	2.0±0.4 amperes
Power	55 watts maximum
Output	
Voltage (To Modular Cooler Motor)	115±19 volts ac, 400 Hz, 2 phase square wave. (capacitor shifted 2nd phase)
Voltage (To System Cooling Fan Motor if required)	24 volts pp (12 Vrms) 400 Hz square wave (0 to 24 Vpp)
Power (To Modular Cooler)	44 watts maximum
Turn-on Time Delay	5±0.2 seconds
Overload Shut-down Time Delay	11±3 seconds

NOTE

For mechanical specifications involved with interface requirements such as mechanical configuration, interconnection and mounting information, refer to section III

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The DC/AC Inverter assembly converts 24 volts dc into an overload protected 115 Vac, 400 Hz, 2-phase power for the universal drive motor in the externally connected Modular Cooler assembly. When interfaced together, the DC/AC Inverter and Modular Cooler assemblies form the Cooler/Inverter common module which is designed to provide the cooling necessary to maintain the detecter array of the Detector/Dewar common module at a temperature of approximately 77° Kelvin.

The DC/AC Inverter is comprised of two interconnected printed wiring boards (A1 and A2) and a heat sink assembly (A3) housed in a metal box for shielding. The square wave generator board (A1) provides the signal generation, shaping and amplification of the 400 Hz square wave used to drive the inverter transistors and also contains the current overload protection circuit. The 24 volt power board A2 and heat sink assembly A3 provide the power drive inverter output circuits and the starting capacitor switch circuit. The output power inverter transistors and phase control capacitors are mounted on the heat sink assembly A3 and the remaining circuitry on A2.

2.2 THEORY OF OPERATION

2.2.1 SQUARE WAVE GENERATOR CIRCUITS (Figure 2-1)

2.2.1.1 Reverse Polarity Protection

The 24 volt dc power entering the DC/AC Inverter assembly is applied to the internal circuits through diode CR1 mounted on the assembly baseplate. Diode CR1 protects the circuits from an accidental reverse polarity input. The input power through CR1 is applied to the square wave generator circuit

AD-A118 049 MAGNAVOX GOVERNMENT AND INDUSTRIAL ELECTRONICS CO MA--ETC F/G 9/5

PRELIMINARY COMMON MODULE DESIGN HANDBOOK.(U)

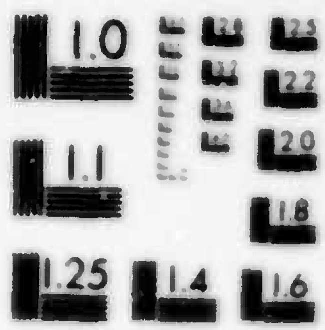
APR 76 DAAG53-75-C-0178

UNCLASSIFIED GSDR-900 NL

3 OF 5

AD A118049

1804



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

NOTES

1. Reference Designator Prefix A1
2. Transistors are 2N222A
3. Resistors are 1/8 W
4. Mounted on Assembly baseplate

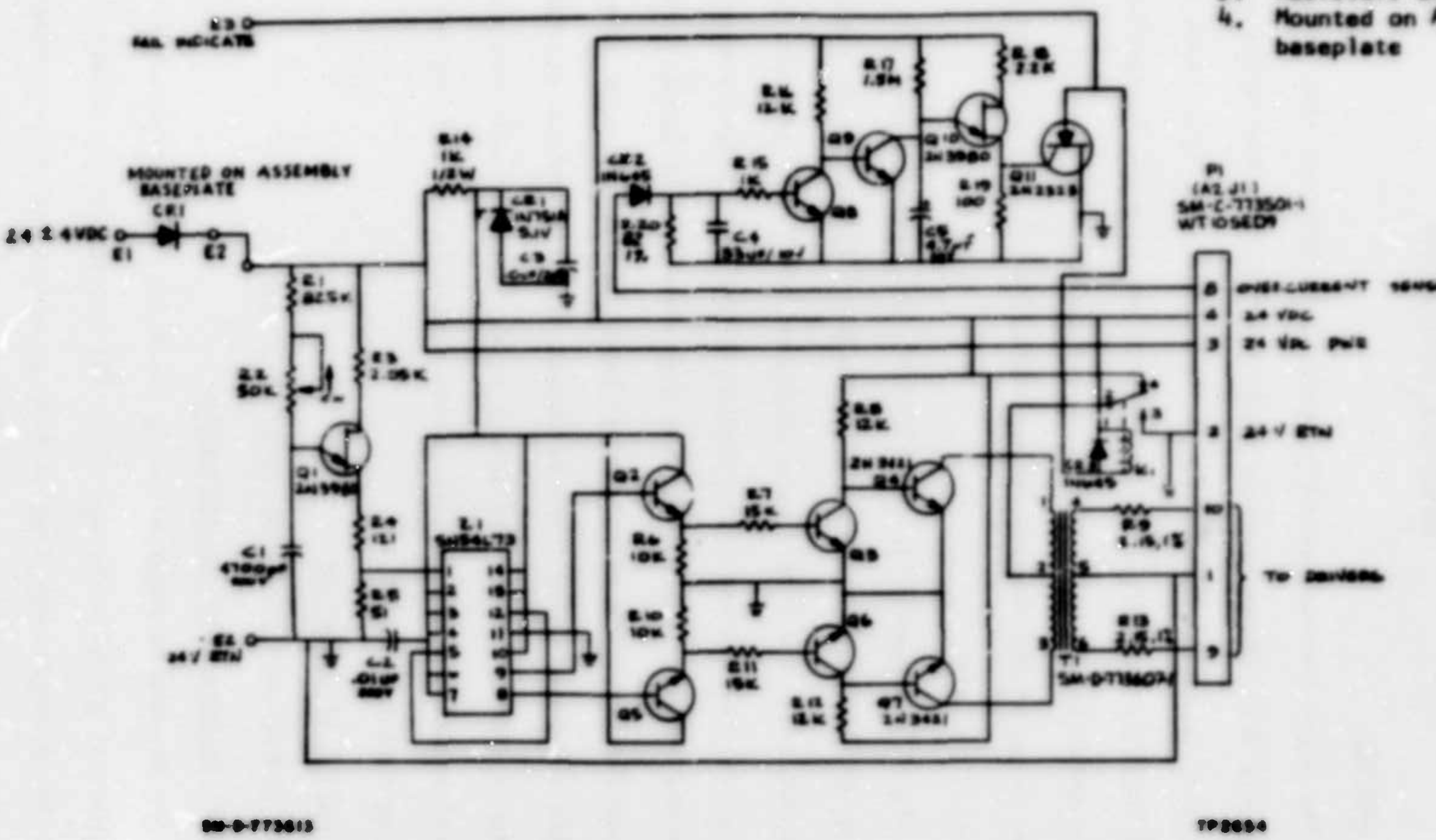


Figure 2-1. Square Wave Generator Circuit Board Schematic Diagram

board A1 and also fed directly through A1 to the 24 volt power board A2 through connector pins P1-3 and 4.

2.2.1.2 Oscillator and Driver Circuits

The 24 volts dc input power is applied to an RC network comprised of capacitor C1, resistor R1 and potentiometer R2. Potentiometer R2 provides frequency control and is adjusted to cause the oscillator unijunction transistor Q1 to oscillate at a frequency of 1600 Hz. The output of Q1 is applied across voltage divider resistors R4 and R5. The positive pulse at the junction of R4 and R5 is applied to the clock input (pin 1) of dual J-K master slave flip-flop Z1. Resistor R14 and zener diode CR1 provide the +5 volts for Z1. The two cascaded flip-flops within Z1 divide the 1600 Hz signal by four to produce a 400 Hz square wave at the second flip-flop outputs (Q at Z1-9 and Q at Z1-8). The outputs of Z1 are 180° out of phase and are applied to the bases of push-pull emitter follower buffer transistors Q2 and Q5. The outputs of Q2 and Q5 are applied to the two stage push-pull driver amplifier transistors Q3, Q4 and Q6, Q7. The collectors of the final stage, Q4 and Q7, drive the primary winding of driver transformer T1. Bias is provided by applying the 24 volts dc input power to the center tap of T1 (pin 2) through the deenergized contacts of relay K1.

The square wave voltage is developed in T1 as follows: On the first one-half cycle, transistors Q2, Q3 and Q4 are turned on by Z1-pin 9. Transistors Q5, Q6 and Q7 are off. Current flows through T1 pin 1 to pin 2 and is returned through the 24 volts dc, developing magnetic flux in one direction in T1. On the next one-half cycle Q2, Q3 and Q4 are turned off and Q5, Q6, Q7 are turned on. Current now flows through T1 from T1-3 to T1-2 developing magnetic flux in the opposite direction. This action developes a square wave flux in the windings of T1. The resultant square wave voltage

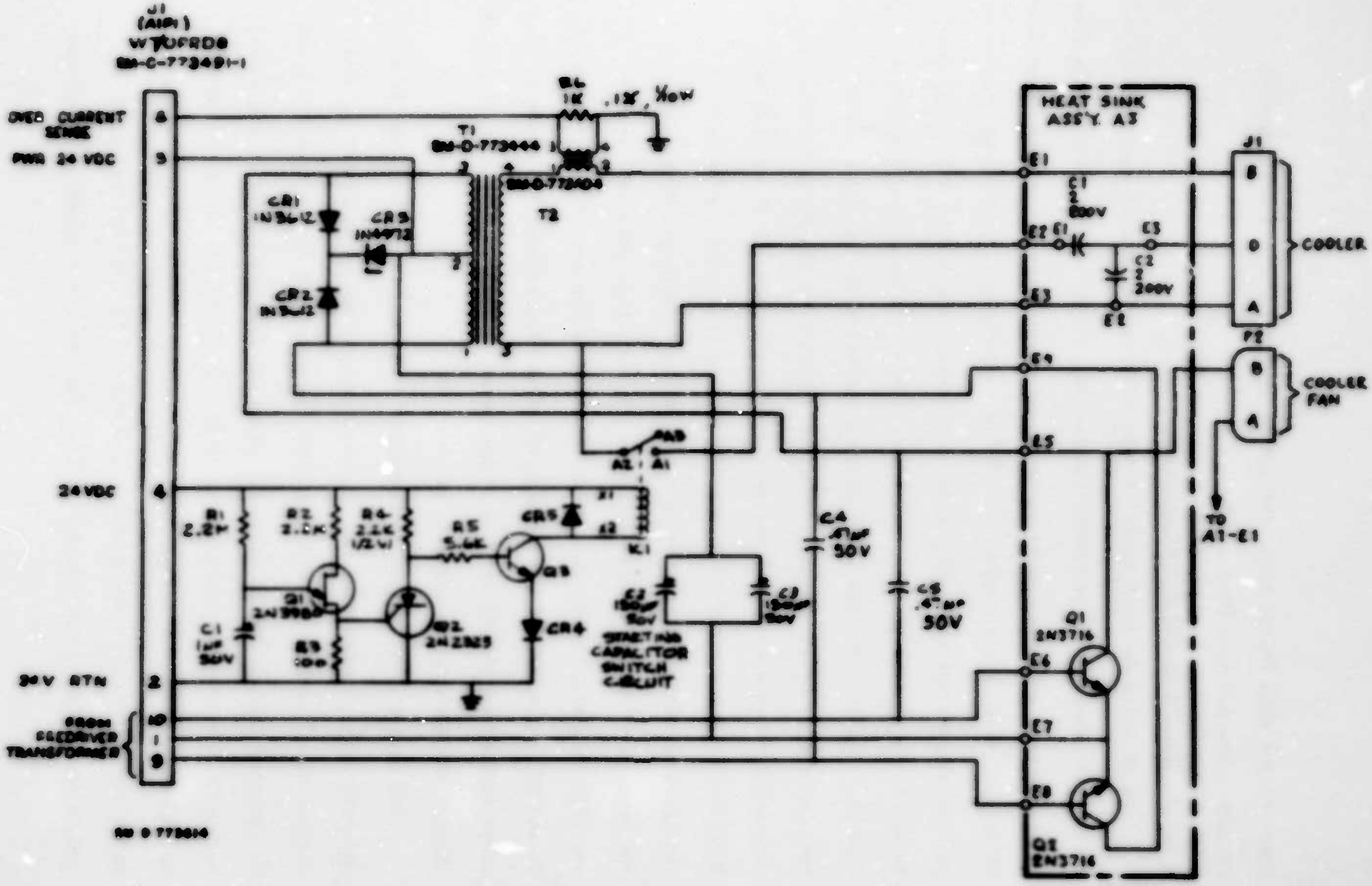


Figure 2-2. 24V Power Board (A2) and Heat Sink Assembly (A3) Schematic Diagram

developed in the secondary of T1 is applied to the power inverter circuit on the 24 Vac power board through connector pins P1-1, 9 and 10. The power inverter circuit will be described in a later paragraph.

2.2.1.3 Current Overload Circuit

Transformer T2 and resistor R6 on the 24 volt power board A2 (Figure 2-2) act as the overload sensor for the overload protection circuit. The current through T2 developes an ac voltage across R6 which is fed to the overload protection circuit on the square wave generator circuit board A1 through connector pin J1-8.

The overcurrent sense voltage entering the circuit through connector pin P1-8 on A1 (Figure 2-1) is half-wave rectified by diode CR2. The rectified dc voltage startsto charge capacitor C4. Under normal operating conditions, the voltage level from CR2 is not high enough to charge C4 to a level that will turn transistor Q8 on. With Q8 off, transistor Q9 is on, and Q10 and Q11 are off. However, if an overcurrent condition developes, the overcurrent sense voltage will increase and C4 will charge to the level required to turn Q8 on. With Q8 on, transistors Q9 starts to turn off and capacitor C5 starts to charge. If the overcurrent condition fails to continue, the positive level is removed from Q8, turning Q8 off and Q9 on, discharging C5 and keeping Q10 and Q11 off. The time constants of the circuit are such that the overcurrent condition must exist for from 8 to 14 seconds before C5 can charge to a level that will turn Q10 on. When the overcurrent condition is sustained for from 8 to 14 seconds, C5 charges up until the base of Q10 becomes forward biased turning Q10 on. When Q10 turns on, thyristor Q11 turns on energizing relay K1 and removing the 24 volts dc from the inverterdriver circuits thereby shutting down the inverter. In addition, a fail indicate signal is made avalloble at terminal A1-E3 that

may be used for a remote fail indicator light or to shut down other modules of the system. Once activated, the shut down condition will be maintained until the input power is cycled off and on .

2.2.2 24 VOLT POWER BOARD CIRCUITS (FIGURE 2-2)

NOTE

> The circuit descriptions provided in this paragraph include components mounted on heat sink assembly A3 as well as those mounted on the 24 volt power board A2.

2.2.2.1 Power Inverter Circuit

The square wave drive signals received from the driver circuit on the square wave generator circuit board A1 through connector pins J1-9 and 10 are applied to the bases of push-pull power inverter transistors Q1 and Q2 mounted on heat sink assembly A3. The return on J1-1 is connected to the common emitters of Q1 and Q2 and the center tap of inverter power transformer T1. The output drive signals on the collectors of Q1 and Q2 are applied across the primary of T1. Diodes CR1, CR2 and CR3 across the primary of T1 act to limit the voltage excursions and switching spikes on the signal. Capacitors C2 through C5 provide additional filtering.

Power transformer T1 acts in the same manner as transformer T1 on circuit board A1 previously described. When Q1 is conducting and Q2 is off, magnetic flux is developed in the top half of the T1 primary winding in one direction. On the other one-half cycle when Q2 is conducting and Q1 is off, the magnetic flux is developed in the lower half of the T1 primary winding in the opposite direction. The nominal 115 Vac, 400 Hz square wave output voltage developed in the secondary winding by the magnetic flux is sent to pins A and B of the cooler connector J1. Capacitors A3 C1 and A3 C2 act as the phase shift capacitors to provide the second phase at cooler connector pin J1-D. Capacitor A3 C1 is added in parallel with A3 C2 as a starting capacitor at

initial turn-on and then disconnected after approximately 5 seconds by the starting capacitor switch circuit as described in the following paragraph.

2.2.2.2 Starting Capacitor Switch Circuit

When the 24 volt dc power to the DC/AC inverter is initially turned on, initial circuit conditions are as follows: transistor Q1 and thyristor Q2 are off and transistor Q3 is on. With Q3 on, starting capacitor switching relay K1 is energized connecting starting capacitor A3C1 in parallel with phase shift capacitor A3C2 through the energized contacts of K1. Simultaneously, at turn on the 24 volts dc is applied to the RC timing network formed by resistor R1 and capacitor A2C1. The RC time constant is such that, after approximately 5 seconds, capacitor A2C1 is charged to the dc level required to forward bias Q1. With forward bias, Q1 turns on enabling the gate of thyristor Q2, turning Q2 on. With Q2 on, the base of Q3 is reverse biased turning Q3 off and deenergizing relay K1 and disconnecting starting capacitor A3C1 from the phase shift circuit. Thus, for initial starting, A3C1 and A3C2 are connected in parallel providing a phase shift capacitance of 4 uf. After approximately 5 seconds relay K1 is deenergized disconnecting A3C1 and leaving A3C2 to provide a running phase shift capacitance of 2 uf.

A 0(zero) to 24 volt peak-to-peak square wave (12 Vrms) voltage is available at the cooler fan connector P2 to supply power for the motor of a system cooling fan if one is required by the system design.

SECTION III

INTERFACE

3.1 CONFIGURATION

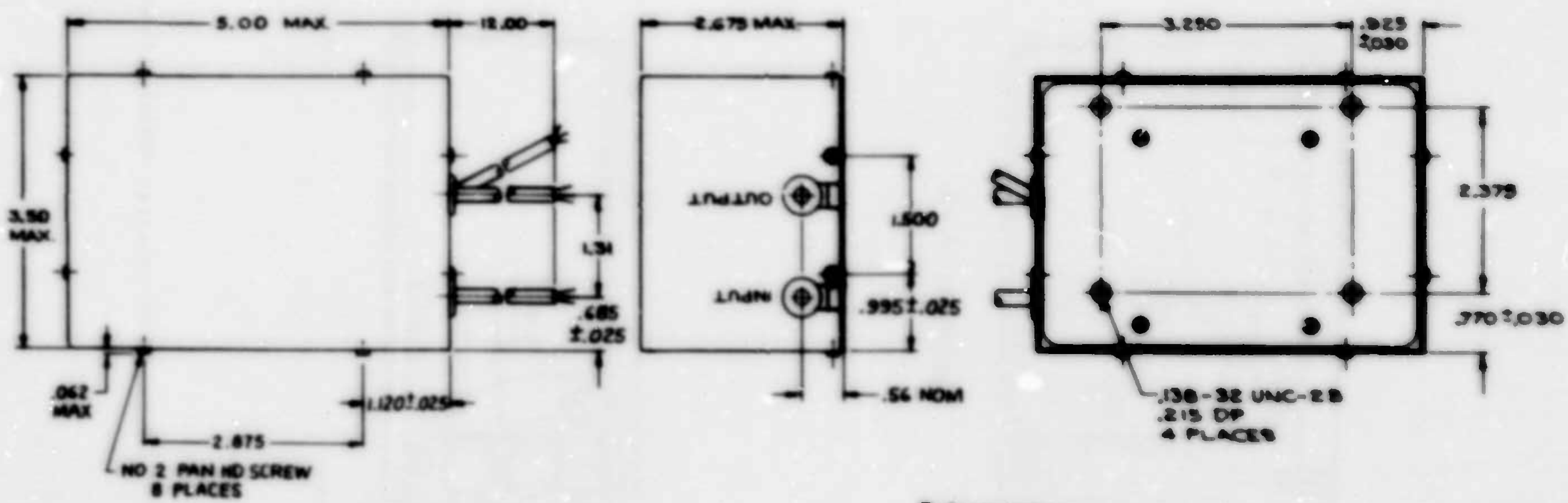
Outline drawing, Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating the DC/AC Inverter modules in a system layout. Note that the dimensions and tolerences reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is the DC/AC Inverter assembly drawing.

3.2 INTERCONNECTING INFORMATION

The DC/AC Inverter is mounted on a flat using four #6-32 screws. The screws shall be of such length as to extend into the DC/AC Inverter no more than .210 inch beyond the base mounting surface. It can be operated in any attitude. Electrical connections are made through three cables which are supplied twelve inches long. The cut lengths of the three cables and the connectors for input and 24 volts output are to be determined by the particular system designer. The connector for the output to the cooler motor must be P/N SM-C-773505-2 to mate with the connector on the motor. This connector is very fragile, so care must be exercised in engaging it and in tightening the screw which holds it to the motor assembly. Also this motor cable should be clamped at some point near the motor to prevent stressing the connector and the wire leads to it by handling or vibration.

The DC/AC Inverter is one of the main heat dissipating modules, so mounting of it must take into consideration the heat transfer requirements discussed in the section on thermal design.

The Inverter has built-in overload protection which shuts it down if an excessive current is dawn by the motor. There is no built-in protection for internal faults in the inverter itself, so the system designer may wish to provide an external circuit breaker on the input power lines.



Tolerances:
.xx = ± .02
.xxx = ± .010

Figure 3-1 DC/AC Inverter Assembly Outline Drawing

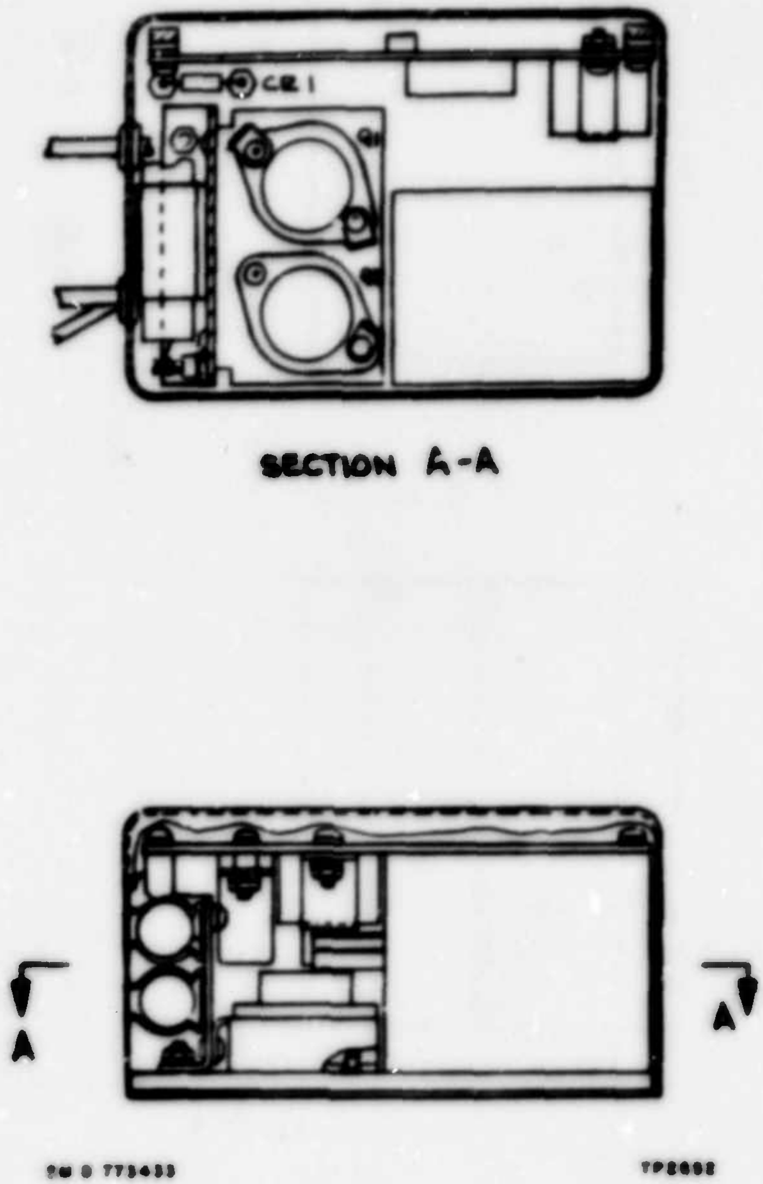


Figure 3-2. DC/AC Inverter Assembly Drawing

3.3 THERMAL DESIGN CONSIDERATIONS

The DC/AC Inverter dissipates approximately 11 watts and is second only to the Modular Cooler in power dissipation in a common module system. This significant thermal power dissipation must be taken into account when designing a common module infrared system. Refer to Section III of Chapter 1 for a detailed discussion of the system thermal design considerations.

3.4 ELECTRICAL INTERFACE DATA

3.4.1 INPUT CHARACTERISTICS

(a)	Voltage	24±4 volts dc
(b)	Current	2.0±0.4 amperes
(c)	Power	55 watts maximum
(d)	Turn-on Time Delay	5±0.2 seconds

3.4.2 OUTPUT CHARACTERISTICS

(a) To Modular Cooler

Voltage	115±19 volts ac, 400 Hz 2-phase square wave, (capacitor shifted 2nd phase)
Power	44 watts maximum
Overload Shut-down Time Delay	11±3 seconds

(d) System Cooling Fan

Voltage	24 volts pp (12 Vrms), 400 Hz square wave (0 to 24 Vpp)

3.4.3 ANCILLARY ELECTRICAL DESIGN CONSIDERATION

(1) Since the input power leads to the Cooler coming from the Power Board terminals E1, E2 and E3 (see schematic diagram Figure 2-2) deliver 115 volt 400 Hertz voltage (approximately 45 watts), these leads should not be routed adjacent to or bundled together with, other leads. Doing so may induce unwanted signals in the other leads. For a like reason, leads from terminal E4 and E5 (48 volt square wave) should be kept apart from other leads.

(2) Since the Inverter dissipates approximately 11 watts (approximately 55 watts input, 44 watts output), it should not be located near or adjacent to heat sensitive piece parts or assemblies.

(3) Since terminal E1, E2, E3 carry a potential of 115 volts and are potentially dangerous to personnel these terminals should be protected by barriers or guards such that accidental contact cannot be made with these terminals. The barrier or guards should be marked "115 volts"

(4) With the maximum input of 28 volts dc, resistor R14, 1000 ohms ±5 percent, 0.5 watt (see schematic diagram Figure 2-2), will operate extemely hot since it can be dissipating anywhere from 0.499 watts to 0.552 watts (overstressed)

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the DC/AC Inverter Module, a component of the Cooler/Inverter Module. Presented herein are the test equipment requirements, test set up, adjustment and alignment techniques.

4.2 TEST EQUIPMENT

The following, or equivalent, test equipment is required to perform the necessary operational tests, alignments, and adjustments on the DC/AC Inverter Module.

4.2.1 STANDARD TEST EQUIPMENT

Table 4-1, following, presents a listing of commercially available equipment which has been found to be adequate for testing of this module.

Table 4-1

Equipment	Manufacturer	Model
Power Supply	Power Design	3650S
Oscilloscope	Tektronics	326
Digital Multimeter	Fluke	8000A
Stop Watch	Edmund Scientific	30371

4.2.2 SPECIAL TEST EQUIPMENT

Convenient means of interconnecting the various equipment used in testing the DC/AC Inverter Module may be achieved by fabricating a test set. Such a test set may be fabricated from the information in Figure 4-1.

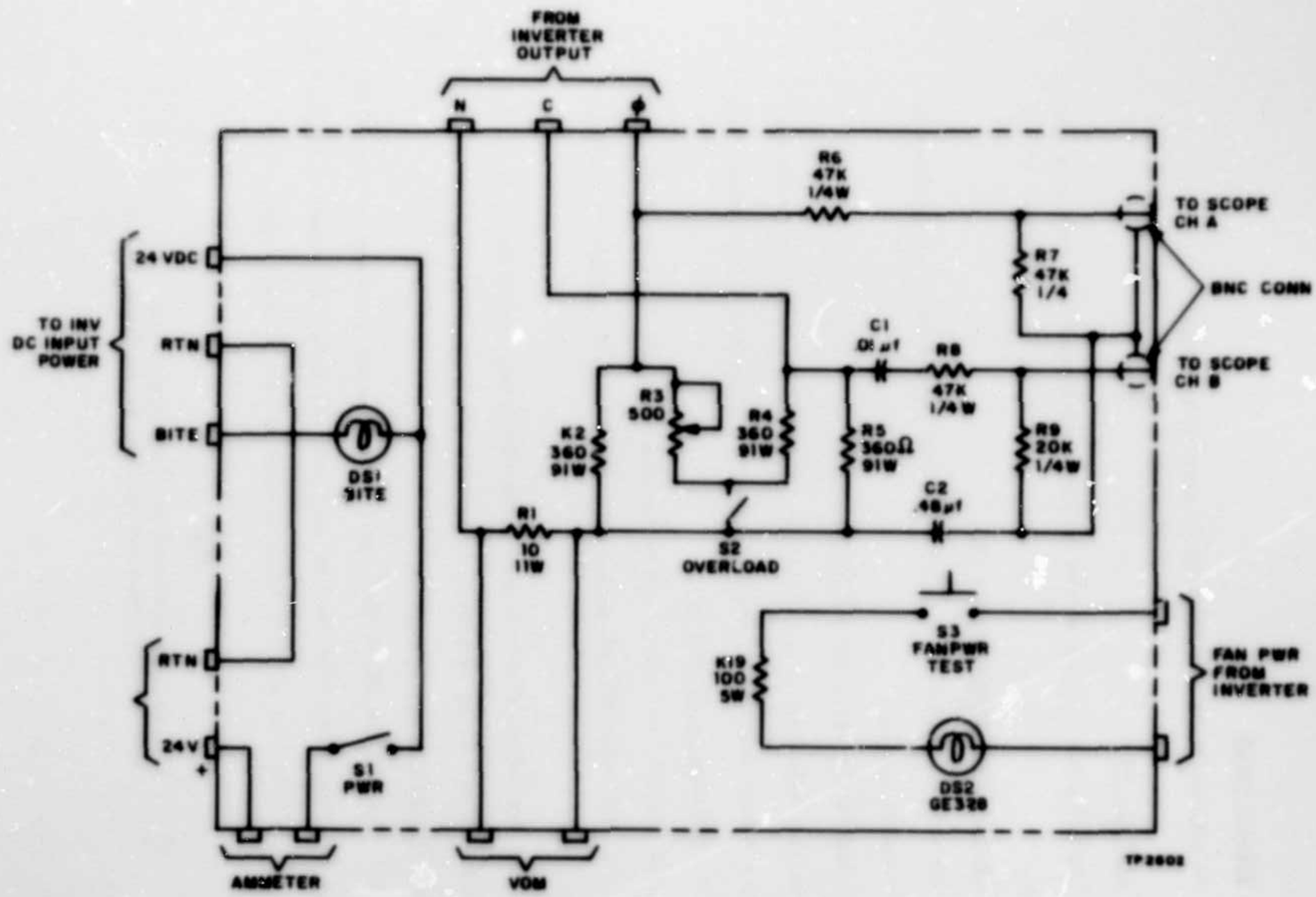


Figure 4-1 DC/AC Inverter Assembly Test Set

4.3 SPECIAL TOOLS

No special tools are required to test this module.

4.4 TEST SET UP

Figure 4-2 is a diagram of the typical interconnections used in a test set up.

4.5 CALIBRATION/PREPARATION FOR USE

Operational status of the DC/AC Inverter Module may be determined by the following tests.

4.5.1 ELECTRICAL TESTS AND ADJUSTMENTS

Perform each test of the following paragraphs in the order presented. Verify a proper response or indication before proceeding to subsequent actions.

4.5.1.1 Calibration of Test Set

4.5.1.1.2 Apply 110 volts, 400 Hz between terminals N and 0 (N is neutral)

4.5.1.1.3 With the OVERLOAD switch OFF, the AC voltage across R1 shall be 4.0 ±0.5 Vac.

4.5.1.1.4 Set OVERLOAD switch to ON; the AC voltage across R1 shall be 7.5 ±0.2 VAC. (Adjust R3 as necessary to achieve the proper voltage).

4.5.1.2 Equipment Interconnection

4.5.1.2.1 Connect the DC/AC Inverter to the test set as shown in Figure 4-2.

4.5.1.2.2 Interconnect the test set and test equipment as shown in Figure 4-2.

4.5.1.2.3 Verify that all the above connections are properly made.

NOTE:

If a battery operated oscilloscope is not used, oscilloscope ground must be isolated.

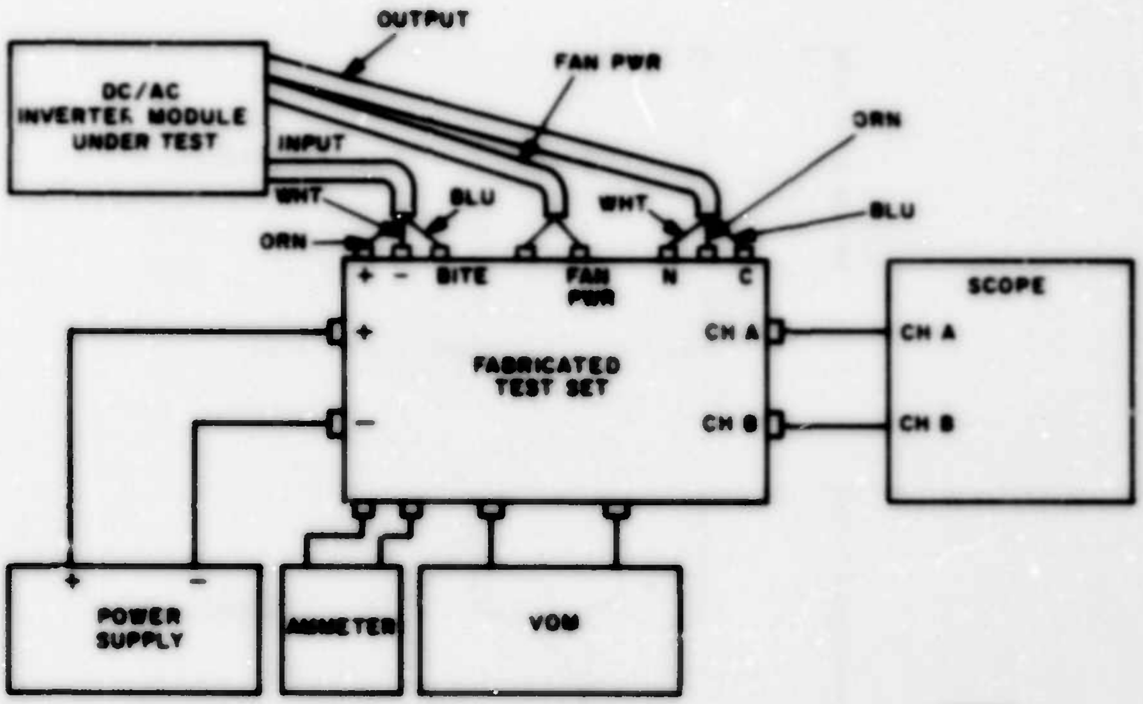


Figure 4-2 DC/AC Inverter Test Setup

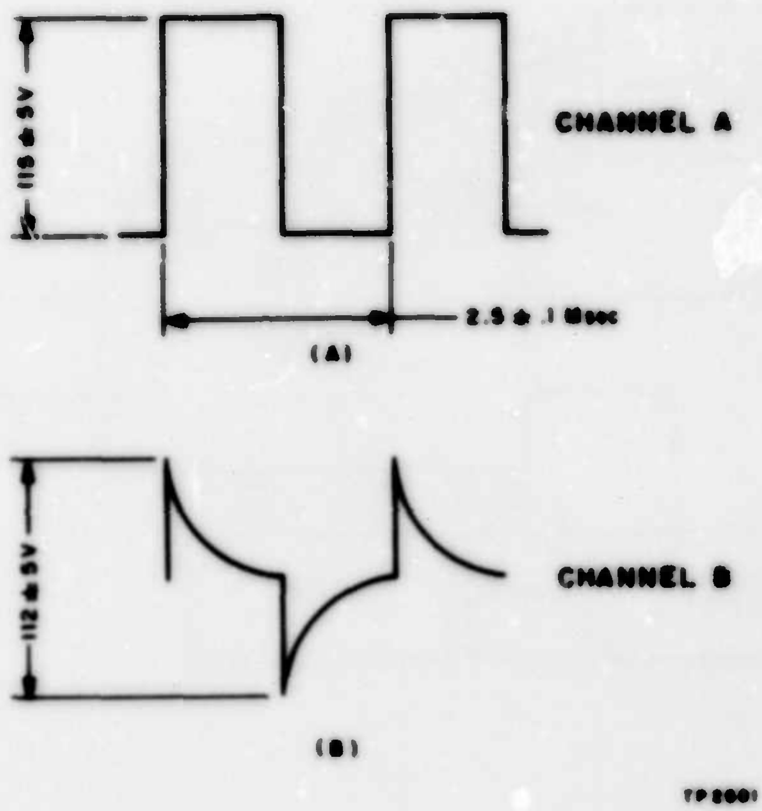


Figure 4-3 DC/AC Inverter Waveforms

4.5.1.2.4 Turn on the power supply and adjust the output to 24 ±1 VDC. Set the power supply current limit for 5 amps.

4.5.1.2.5 Set the oscilloscope controls as follows:

Channel A	20 volts/division
Channel B	20 volts/division
Time/Div	0.5 milliseconds

4.5.1.2.6 Set the digital multimeter to ACV, 20 volt range.

4.5.1.3 <u>Start Up Time</u>

Set the test set POWER switch to ON and simultaneously start the stop watch. Note the time required for the input current to drop below 3 amps.

The elapsed time shall be 5.0 ±2.0 seconds.

4.5.1.4 <u>Output Waveforms</u>

The DC/AC Inverter output waveform shall be as shown in Figure 4-3

4.5.1.5 <u>Fan Power</u>

Depress the test set FAN POWER switch momentarily.

The test set FAN POWER TEST light shall illuminate.

4.5.1.6 <u>Overload and BITE</u>

4.5.1.6.1 Set the test set OVERLOAD switch ON and simulataneourly start the stop watch. Note the time required for the output signals displayed on the oscilloscope to drop to zero.

The elapsed time shall be 11 ±3.0 seconds.

The BITE light shall eliminate when the signals drop to zero

4.5.1.6.2 Note the reading on the digital meter.

The voltage shall be 10.0 ±0.5 VAC.

4.5.1.6.3 Set the OVERLOAD switch to OFF.

The BITE light shall remain eliminated.

4.5.1.6.4 Set the test set POWER switch OFF momentarily and then return to ON.

The BITE light shall extinguish and normal operation shall be restored.

4.5.2 MECHANICAL ALIGNMENT

No mechanical alignment is required for the DC/AC Inverter.

4.5.3 ADJUSTMENT IN THE SYSTEM

When installed in a system, the DC/AC, Inverter is sealed and no adjustments are required.

4.6 SPECIAL MAINTENANCE

The DC/AC Inverter module requires no special maintenance attention beyond the routine procedures followed for general electric equipment. No time change components are contained in this module.

CHAPTER 7

MODULAR COOLER

USAECOM SM-D-773683

PART OF

COOLER/INVERTER, INFRARED MODULE

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

1.1.1 COOLER/INVERTER, INFRARED

The Cooler/Inverter, Infrared common module is comprised of two separately functioning assemblies; the Modular Cooler Assembly and the DC/AC Inverter Assembly. This section of the manual describes the functioning and provides design information on the Modular Cooler. The DC/AC Inverter is described in Chapter [illegible] of the manual.

1.1.2 MODULAR COOLER

The Modular Cooler Assembly is a Stirling cycle cryogenic refrigerator capable of maintaining a temperature of approximately 77°Kelvin at the cold finger with a heat load of 1.0 watt. The modular cooler provides the cooling necessary for proper operation of an externally connected infrared detector array. The detector array is contained in a common or special Detector/Dewar module which is mechanically interfaced with the cold finger of the modular cooler.

1.2 INTENDED USE OF ITEM

The Modular Cooler has been designed to be interfaced with other major common and special modules to form an integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The Modular Cooler has been specifically designed to be mechanically and thermally interfaced with a detector/dewar module to provide the cooling required to maintain the infrared detector array at approximately 77° Kelvin.

The Modular Cooler is designed primarily to be integrated into a system as part of the Cooler/ Inverter common module with the Modular Cooler supplying

the required cooling for a detector array and the DC/AC inverter supplying 115 Vac, 400 Hz power for the cooler motor. However, the Modular Cooler may also be designed into a system as a separate module without the DC/AC inverter if some other suitable 115 Vac, 400 Hz power source is available to drive the cooler motor.

1.3 TECHNICAL SPECIFICATIONS

The technical specifications for the Modular Cooler are as follows:

Parameter	Specification
Cool down Time (600 joule thermal mass plus heat input ranging from zero when starting to 0.4 watt at cold finger temperature of 77° K.)	10 minutes maximum to 100° Kelvin 15 minutes maximum to 77° Kelvin
Input	
Voltage	115 ± 19 Vac, 400 Hz, 2 phase
Power	44 watts (nominal)
Cooling Capacity (watts)	1 watt from -60° to +23°C ambient dripping linearally from 1 watt at 23°C to 0.4 watt at 80°C

NOTE

For technical specifications involved with interface requirements such as mechanical configuration, interconnection and mounting information, refer to Section III.

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The Modular Cooler assembly is a Stirling-cycle cryogenic refrigerator driven by an AC drive motor. 115 Vac, 400 Hz, 2-phase power for the drive motor is usually supplied by the DC/AC Inverter assembly. The motor may also be driven from any other suitable 115 Vac, 400 Hz power source.

Referring to Figure 2-1, major components of the Modular Cooler are: the drive motor, the compression cylinder and piston, the regenerator and the cold finger. The working fluid in the cooler system is helium gas. The compression piston and regenerator are driven by a common drive motor linked mechanically through the drive rods attached to the crank shaft approximately 90° out of phase.

Threaded mounting holes are provided in the cylinder head as well as in the base. To maintain the specified operating temperature of 77° K (Kelvin) at the cold finger, it is essential that the cylinder head be attached to a suitable heat sink such as a cold plate heat exchanger. For details on the thermal interface requirements, refer to Section III of Chapter 1.

2.2 THEORY OF OPERATION (Figure 2-1)

The Modular Cooler uses helium gas as the working fluid. The gas is alternately compressed and allowed to expand. The compression piston and regenerator are driven by a common drive motor through a crank mechanism with the regenerator motion lagging the piston motion by approximately 90° of crankshaft rotation. Internally, the regenerator contains a matrix or porous mass of fine wire having a large heat transfer capacity to the helium gas. The gas can flow freely back and forth between the compression chamber above the compression

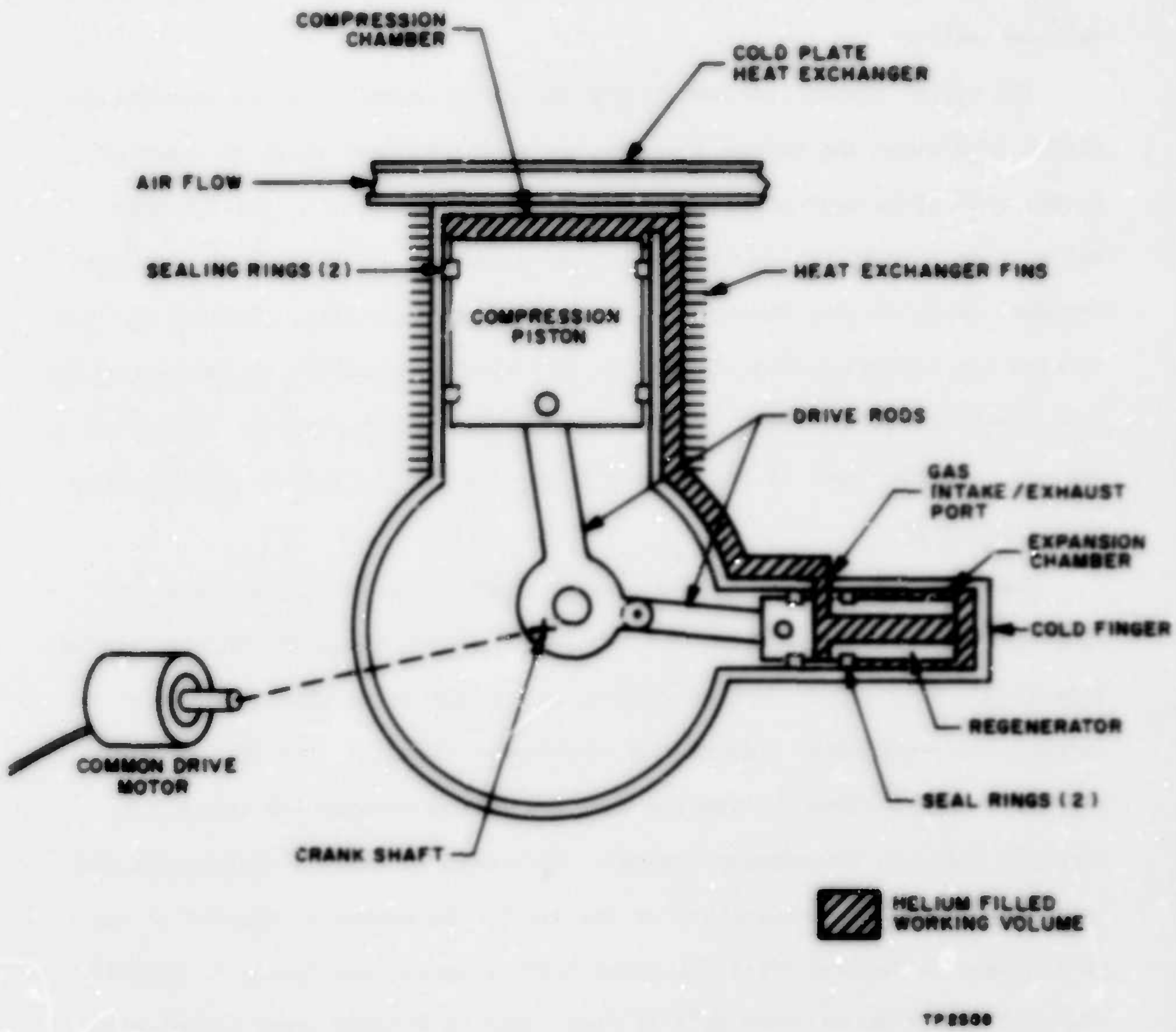


Figure 2-1. Cooler Module Mechanical Diagram

piston and the expansion chamber at the end of the cold finger by flowing through the regenerator matrix and connecting channels in the compression cylinder walls.

The cooler system operates in the following manner. As the compression piston compresses the helium gas, the gas gives off heat which is drawn off by the cold plate heat exchanger (heat sink) and the fins on the cylinder walls. The compression of the gas by the compression piston forces the gas through the connecting channels into the regenerator matrix. As the gas flows through the regenerator matrix towards the expansion chamber at the end of the cold finger additional heat is drawn from the gas by the matrix. Therefore, the gas is colder when it reaches the expansion chamber than it was entering the regenerator.

When the pressure in the compression chamber starts decreasing as the compression piston moves back, the cooled gas in the expansion chamber starts expanding. This causes further cooling of the gas which then flows back through the regenerator towards the compression chamber. The gas now cools the matrix as it flows thruugh the regenerator and through the connecting channels into the compression chamber. With each succeeding compression and expansion cycle, the temperature of the gas in the expansion chamber of the cold finger is reduced until the gross cooling equals the losses ($\approx 77°K$). The cool down time to reach 77°K is from 12 to 15 minutes under normal ambient conditions. Once down to the stable operating temperature, with each cycle the cold finger in thermal contact with the detector/dewar removes any heat generated by the detector array or entering the dewar through thermal leakage.

SECTION III

INTERFACE

3.1 CONFIGURATION

Figure 3-1 (2 sheets) shows the pertinent outline and mounting data for use of the designer in incorporating the Modular Cooler in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is a photograph of the Modular Cooler.

3.2 INTERCONNECTING

The Modular Cooler may be operated in any attitude. There are tapped mounting holes provided both in the base and in the cylinder head. However, it is usually better to use the head mounting surface since it has a closer control of tolerances between this and the cold finger. Also, since good heat transfer from the cooler is essential for its performance, head mounting is preferred as discussed in the section on thermal design.

Since the detector/dewar is rigidly attached to the cooler, their mounting in the system must be accomplished as a unit. A typical design of the cooler mounting involves the use of an aluminum right-angle bracket to which the head of the cooler and the mounting flange of the detector/dewar module are attached. Dowel pins locate the bracket relative to the system structure, which may be a heat exchanger assembly as described in the thermal design section. Within the assembly of the cooler, detector/dewar, and the bracket, adjustments must be provided to compensate for dimensional tolerances in the parts so that the detector elements can be located in a fixed relation to the bracket locating dowels. This permits the cooler-detector assembly with its mounting bracket to be removed and replaced or another assembly to be substituted in the system without need for optical system realignment.

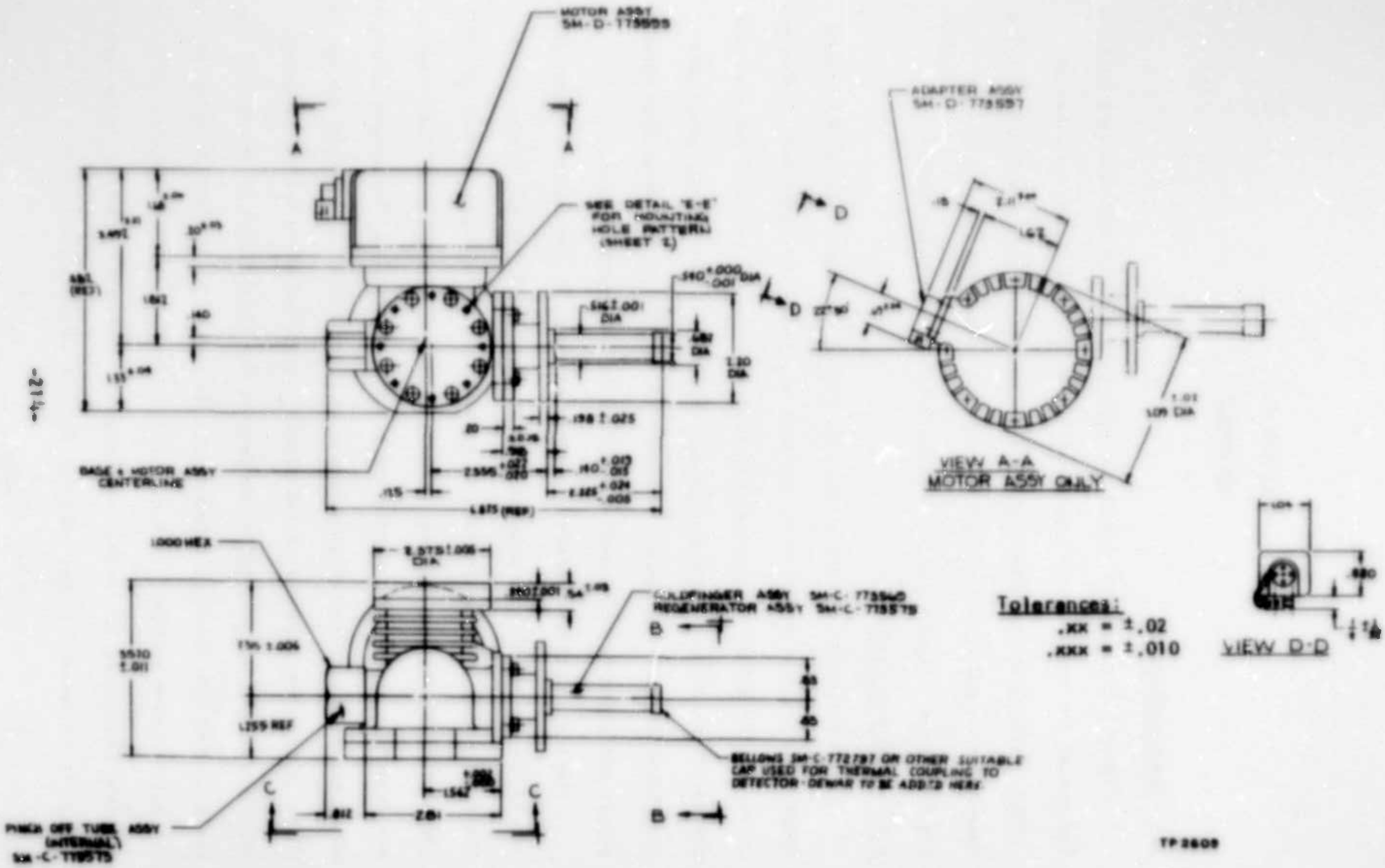


Figure 3-1 Modular Cooler Outline Drawing (Sheet 1 of 2)

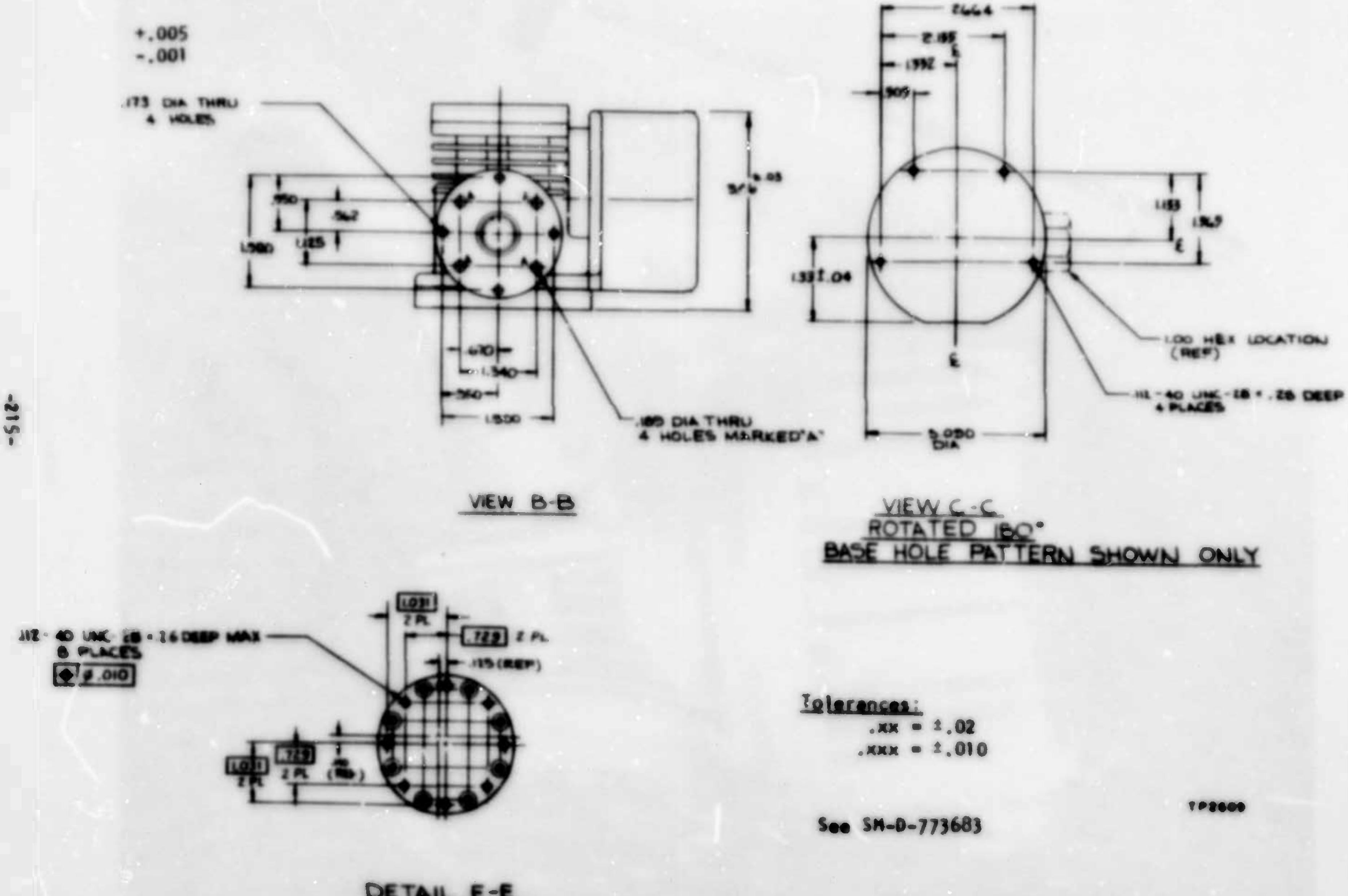


Figure 3-1 Modular Cooler Outline Drawing (Sheet 2 of 2)

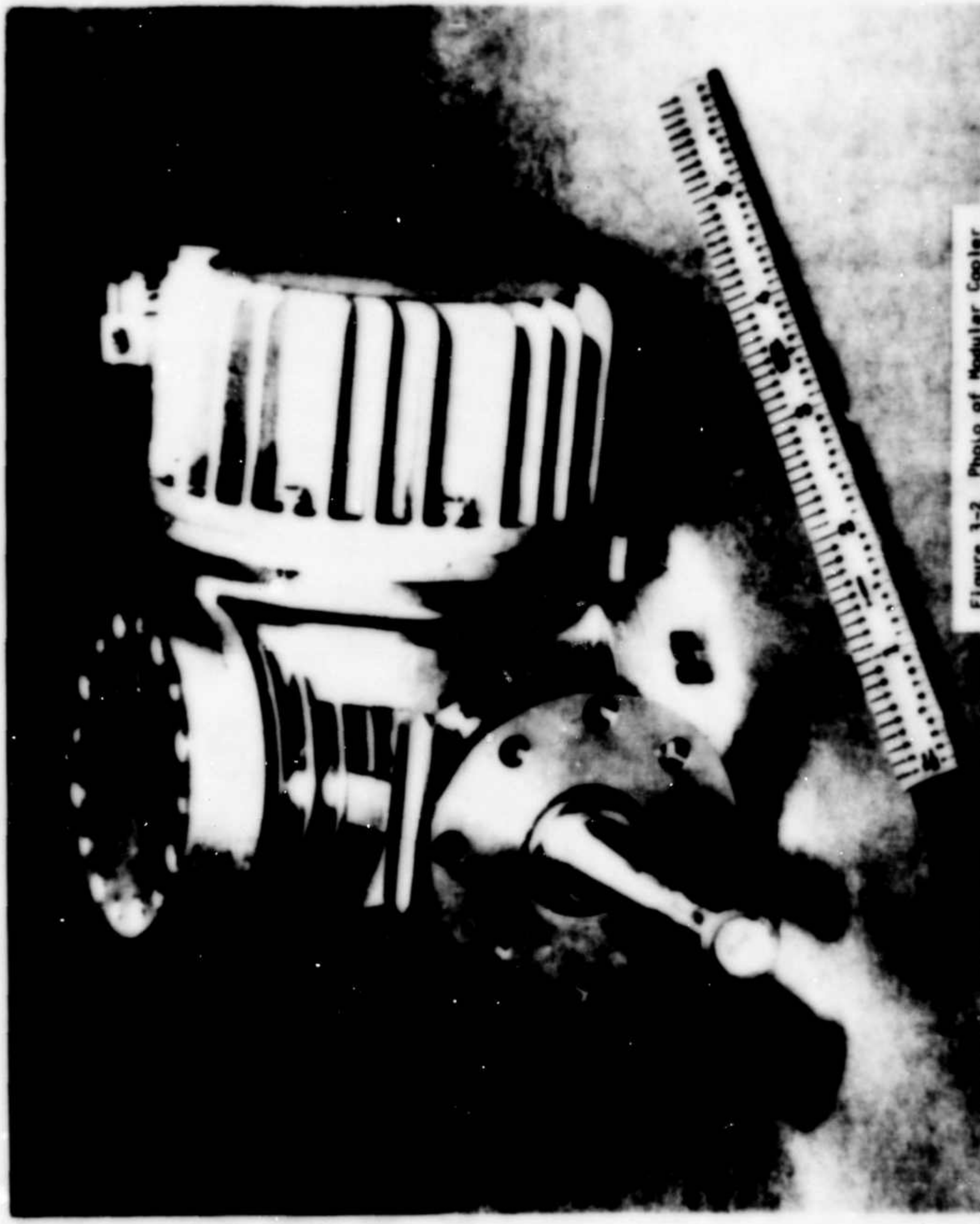


Figure 3-2 Photo of Moduler Cooler

The bracket forms the interface between the cooler head and the heat exchanger. It must be made of a material having high thermal conductivity. Although it imposes a slight added thermal resistance, it aids in distributing the cooler head output into a larger surface area of the heat exchanger, and thereby aids in the over-all head transfer. The cooler power dissipation of 44 watts is divided about equally between the electrical losses in the motor and the mechanical losses due to friction and compression work. In a typical system, about 40 watts are conducted to the heat exchanger with a temperature difference of about 14°C between the cooler cylinder head and the stream of external cooling air through the exchanger. The remaining 4 watts are transferred by radiation and convection to the inside air and housing of the system.

The power connector on the motor is very fragile, so special care must be exercised in tightening the screw holding it to the motor and in engaging the mating connector. The cold finger has a wall only a few thousandths of an inch thick, so extreme care must be used to protect it from damage in handling, packing, and installing. The cold finger is nominally .219 inch shorter than the mating recess in the Detector-Dewar/Bias Pack module (hereafter called Detector module). The extreme range of this clearance is from .176 to .227 inch. To establish thermal contact between the end of the cold finger and the end plate of Dewar recess, on which the Detector is mounted, a bellows (SM-C-772797) is usually used together with a thermal grease. The bellows, filled with thermal grease and with a thin film of the grease on

the end, is placed on the end of the cold finger before mounting the Detector module on the cold finger. Extreme care must be exercised so as not to damage the cold finger or Dewar. The Detector module is held against the cold finger flange by four #6-32 screws threaded into the rear of the Detector module. Note that the Detector-Dewar assembly in the Detector module can be rotated and locked in any angular position in the module as required for any particular system optical layout. This adjustment must be made before assembling the Detector module to the cold finger.

3.3 THERMAL DESIGN CONSIDERATIONS

Of all the Common Modules, the Modular Cooler poses the greatest problem for system thermal design both because it has the highest thermal dissipation (44 watts) and because its detector cooling performance deteriorates at elevated temperatures where its cold finger cooling load is the greatest. For these reasons it has a very significant effect on system thermal design and is discussed in detail in the system "Thermal Design Considerations" (Section III of Chapter 1).

The system can be designed so that there is very little IR defocus caused by thermal expansions within the Cooler, Dewar, and structure. The designer must take into account the average operating temperatures expected in the glass, kovar, stainless steel and aluminum parts which make up the dewar, cold finger, cooler and mounting structure. In a typical system, the focal plane of the detectors may shift about 0.005 inch for an ambient temperature change of 100°F.

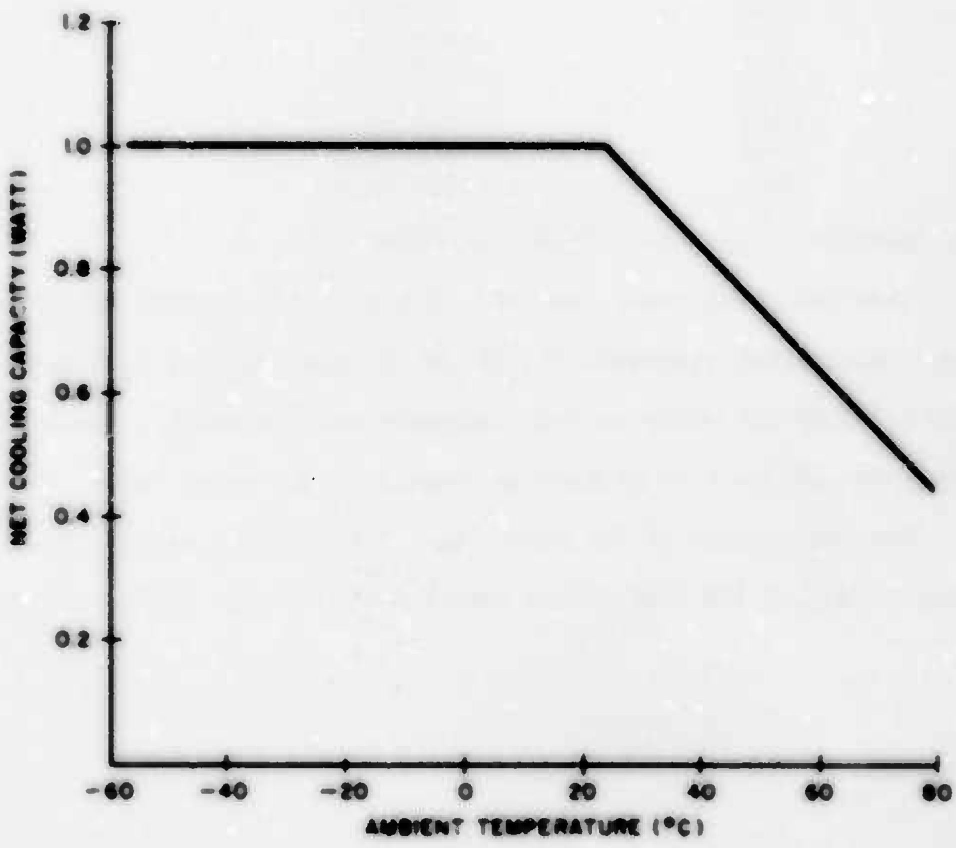
3.4 <u>ELECTRICAL INTERFACE DATA</u>

3.4.1 INPUT CHARACTERISTICS

(a) Power: 55 watts maximum at inverter input and 44 watts maximum at cooler input with a 24.0 ±4.0 volts dc source

3.4.2 OUTPUT CHARACTERISTICS

(a) Cooling capacity: net cooling capacity at 77°K in the ambient temperature range of -60 to +80°C is as follows:



3.4.2 PROCESSING CHARACTERISTICS

(a) Cooldown time: with a 600 joule thermal mass plus a heat load ranging from 0 watt when starting at room temperature to 0.4 watt at 77°K. 10 minutes maximum from turn-on until 100°K is achieved; 15 minutes maximum to achieve 77°K

(b) Audible noise: The specified noise level at a distance of 25 feet is not to exceed the sound pressure levels listed below. The present units do not fully meet this so in applicationswhere low noise is important, consideration should be given to use of acoustic absorption treatment of the cooler or the housing in which it is mounted.

Center frequency (Hz)	Octave band (Hz)	Maximum sound pressure level (dB) Reference 0.0002 microbar
125	87-175	40
250	175-350	39
500	350-700	34
1000	700-1400	32
2000	1400-2800	35
4000	2800-5600	36
8000	5600-11200	34

3.4.4 ANCILLARY ELECTRICAL DESIGN CONSIDERATION

Since the input power leads to the Cooler coming from the DC/AC inverter power board terminals E1, E2 and E3 (see Figure 2.2, Chapter 6) deliver 115 volt 400 Hertz voltage (approximately 44 watts), these leads should not be routed adjacent to or bundled together with, other leads. Doing so may induce unwanted signals in the other leads. For a like reason, leads from terminal E4 and E5 (48 volt square wave) should be kept apart from other leads.

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the Cooler Module. Presented herein are the test equipment requirements, test set up, adjustment and alignment techniques.

4.2 TEST EQUIPMENT

The following, or equivalent, test equipment is required to perform the necessary operational tests, alignments, and adjustments on the Cooler.

4.2.1 STANDARD TEST EQUIPMENT

Table 4-1, following, presents a listing of commercially available equipment which has been found to be adequate for testing of this module.

Table 4-1

STANDARD TEST EQUIPMENT

Equipment	Manufacturer	Model
*Power Supply	Power Design	3650S
Power Supply (2)	Lambda	LPD422B4
Digital Multimeter	Fluke	8000A
Fan	Rotron	M747
Wattmeter, AC	Sensitive Research	VAW
Stop Watch	Edmund Scientific	30371
Vacuum Pump	Welch	Duo Seal 1402
Diode		IN4148

*Not required if 115 VAC, 400 Hz, 1 ϕ, power at 100 watt capacity is available.

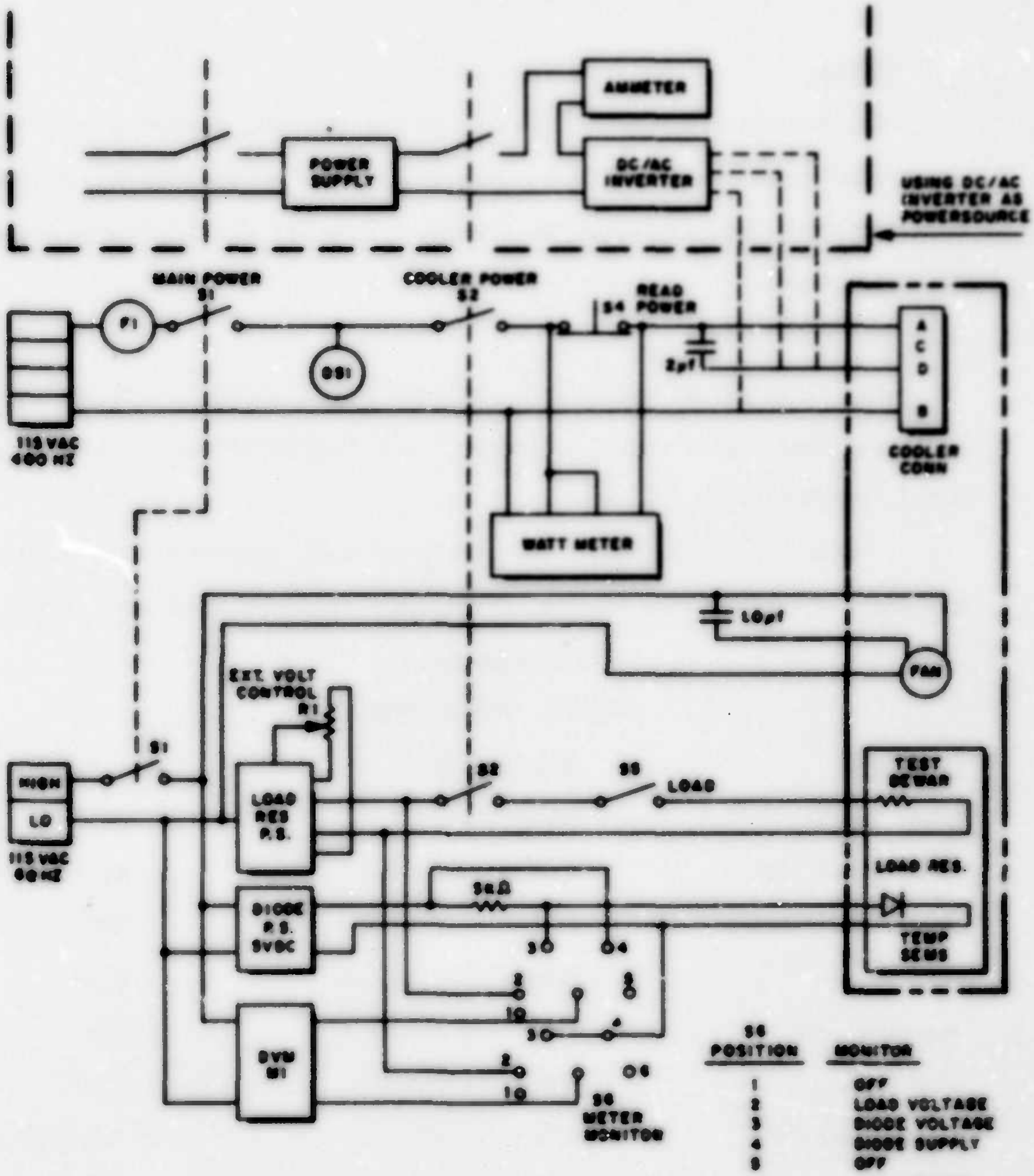


Figure 4-1. Test Set

4.2.2 SPECIAL TEST EQUIPMENT

The special equipment listed in Table 4-2 is required to adequately test the operational status of the Cooler Module.

Table 4-2

SPECIAL TEST EQUIPMENT

Equipment	Manufacturer	Model
*DC/AC Inverter	USA ECOM	SM-D-773433
Cap, Cold Finger Thermal Test	PAVSC/GSD	2002098
Adapter, Cold Finger Thermal Test	PAVSC/GSD	3002101
Test Dewar	PAVSC/GSD	2002219
Mounting Plate	PAVSC/GSD	3002100
Standoff Support	PAVSC/GSD	2002099
Test Set	Fabricate Locally	See Figure 4-1

*Not required if alternate source of 115 V, 400 Hz power is available

4.3 SPECIAL TOOLS

No special tools are required to test this module.

4.4 TEST SET UP

Figure 4-2 is a diagram of a typical test set up

4.5 CALIBRATION/PREPARATION FOR USE

Operational status of the Cooler Module may be determined by the following tests.

4.5.1 CALIBRATE TEMPERATURE SENSOR AND LOAD RESISTOR

4.5.1.1 Connect the temperature sensing diode, IN4148, and the load resistor as shown in Figure 4-3 and secure them to the Cold Finger Cap.

4.5.1.2 Immerse the cap in liquid nitrogen and record the resistance and diode voltage.

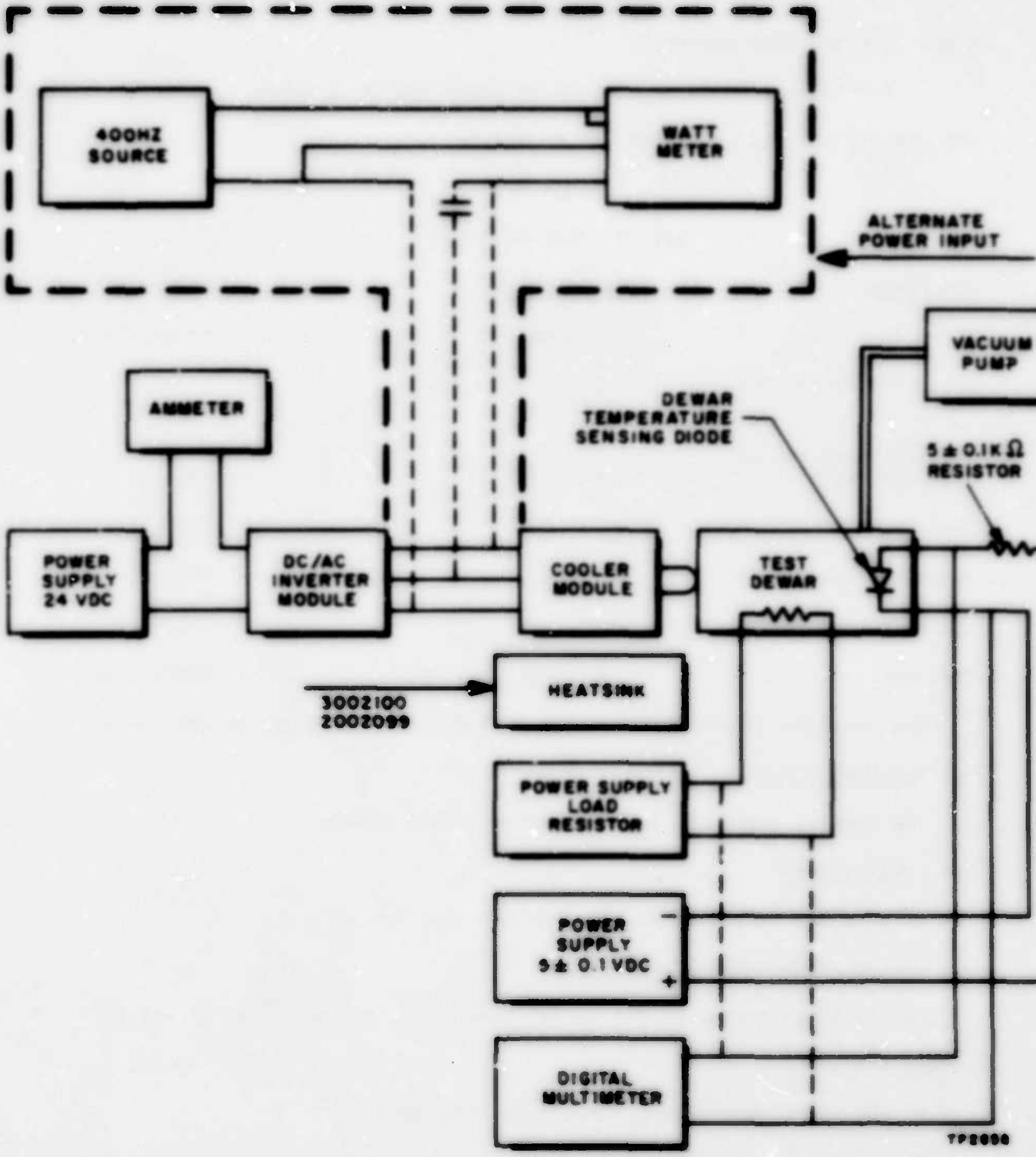


Figure 4-2. Cooler Module Test Setup

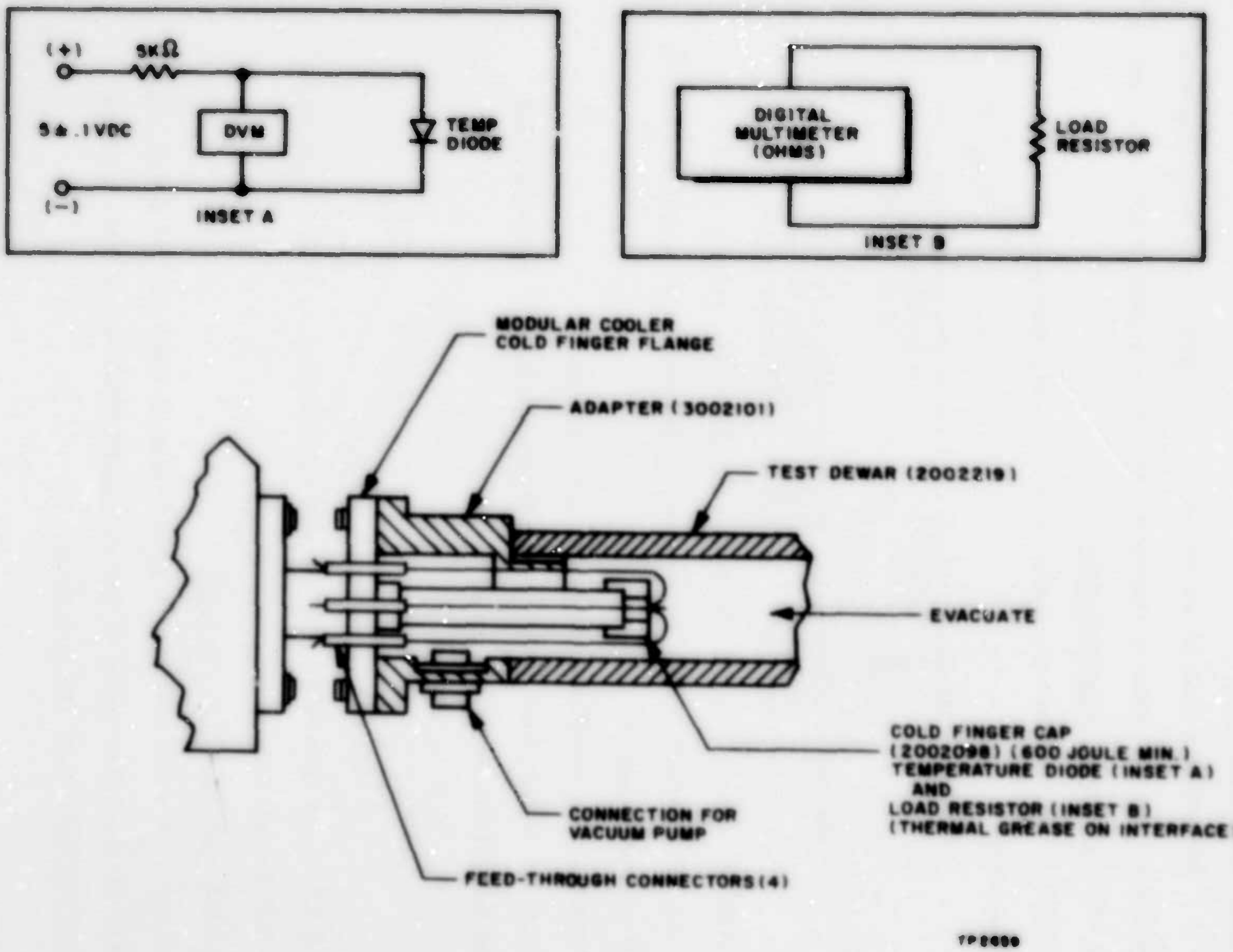


Figure 4-3. Test Set Up

4.5.2 ELECTRICAL TESTS

Perform each test of the following paragraphs in the order presented. Verify a proper response or indication before proceeding to subsequent actions.

4.5.2.1 Equipment Interconnection

4.5.2.1.1 Interconnect the Cooler Module and test equipment as shown in Figure 4-2.

> NOTE: The Cooler Module may also be operated from a single phase, 115 VAC, 400 Hz power source by using a 2.0 Mfd phase shifting capacitor as shown in Figure 4-4.

> CAUTION: Failure to use the proper phase shift with the input power supplied to the Cooler drive motor could result in damage to the Cooler Module

4.5.2.1.2 Verify that all the above connections are properly made.

4.5.2.1.3 Energize the vacuum pump and evacuate the Test Dewar to 1×10^{-3} Tor maximum pressure.

4.5.2.1.4 Set diode power supply to 5.0 ± 1.0 VDC.

4.5.2.1.5 Adjust load resistor voltage to provide a 0.5 watt heat load. The voltage may be calculated as follows:

$$V = \sqrt{.5R}$$

When R = load resistance at 77° K recorded in paragraph 4.5.1.2.

4.5.2.1.6 Set MAIN POWER (S1) and FAN (S3) switches to their ON positions. Direct fan air flow across the Cooler.

4.5.2.2 Cool Down Time (No Load)

4.5.2.2.1 With the equipment interconnected as shown in Figure 4-1; apply power to the Cooler Module by setting COOLER POWER SWITCH (S2) to ON and simultaneously start the stop watch.

4.5.2.2.2 Note the time required for the Cooler to achieve a temperature of 77°K. A temperature of 77°K is indicated by a voltage reading on the digital voltmeter monitoring the diode voltage equal to the reading recorded in paragraph 4.5.1.2.

The elapsed time shall be 15 minutes maximum.

4.5.2.3 <u>Load Test</u>

Set LOAD switch (S5) to ON. Note the diode voltage after 30 minutes operating with the heat load on.

The voltage shall be equal to or greater than the voltage recorded in paragraph 4.5.1.2.

4.5.2.4 <u>Input Power</u>

With the equipment operating as in the previous test momentarily depress READ POWER (S4) switch and note Cooler input power indicated on watt-meter.

Input power to the Cooler shall not exceed 44 watts.

If the DC/AC Inverter is used; input power to the inverter shall not exceed 55 watts.

4.5.2.5 <u>Shut Down Procedure</u>

4.5.2.5.1 Set COOLER POWER switch OFF, and turn off the vacuum pump.

4.5.2.5.2 After approximately 30 minutes turn off test set MAIN POWER and disassemble setup.

<u>CAUTION</u>

> Do not attempt to disassemble the interconnected Cooler, Test Dewar, and vacuum pump until at least 30 minutes after COOLER POWER shut down.

4.5.3 MECHANICAL ALIGNMENT

The Cooler Module requires no mechanical alignment upon installation in a system, other than to provide adequate thermal dissipation paths as

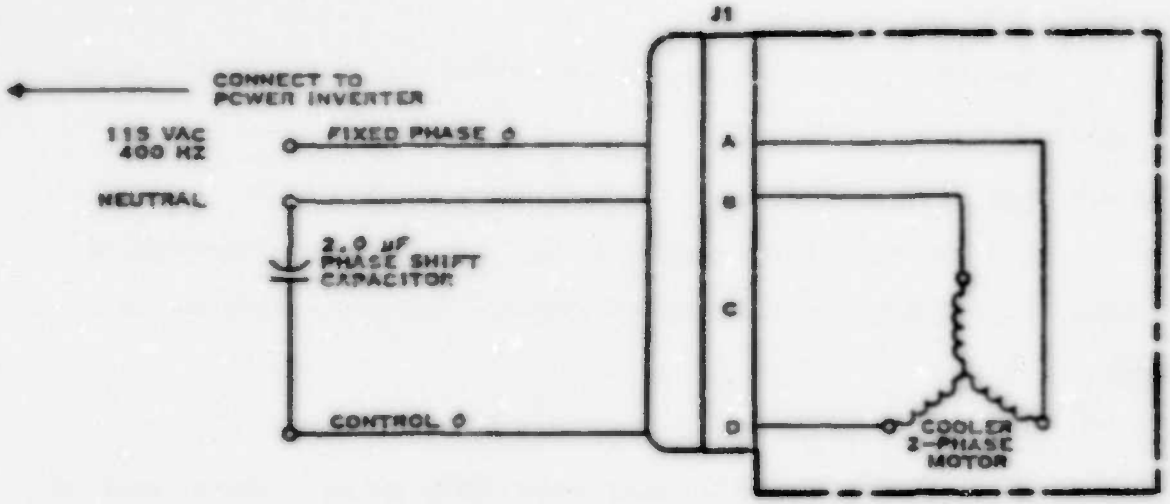


Figure 4-4. Cooler Module Schematic Diagram

discussed earlier in this section.

4.5.4 ADJUSTMENT IN THE SYSTEM

No adjustment of the Cooler Module is required or provided for, when installed in a system.

4.6 SPECIAL MAINTENANCE

The Cooler Module requires some special maintenance attention beyond the routine procedures followed for general electronic equipment. Since no fill port or helium pressure status gauge is provided, it may be advisable to partially disassemble the Cooler after every 500 hours of operation or when the cooling capacity is found to be inadequate.

4.6.1 MAINTENANCE REPLACEMENT ITEMS

When the Cooler has been disassembled, all piston rings and seals must be closely inspected for evidence of wear or deterioration and replaced as necessary.

CHAPTER 8

SCAN AND INTERLACE,

INFRARED (60 Hz)

USAECOM SM-D-773894

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Infrared Scan and Interlace (60 Hz) Module (hereinafter called the Scan and Interlace) differs physically and electrically from, and should not be confused with the Scan and Interlace, Infrared (30 Hz, Low Power) module, P/N SM-D-772111.

The Scan and Interlace module contains the drive electronics to operate and control the Scanner, Mechanical module. The Scanner, Mechanical module contains mirror drive motors, interlace solenoids, a scan position transducer, an interlace position transducer, and a transducer bridge network. The Scan and Interlace module interacts with these elements.

1.2 INTENDED USE OF ITEM

The Scan and Interlace module has been designed to interface with other major common and special modules to form an integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The primary function of the module is to monitor and control the Scanner, Mechanical, which, in conjunction with others modules, optically scans the a thermal image of objective space onto a detector array and simultaneously scans the output of an LED array and collimator to the visual output optics of a system.

1.3 TECHNICAL SPECIFICATIONS

The technical specifications of the Scan and Interlace module are fully described in Development Specification 82-28A050120. Abbreviated specifications are as follows:

Parameter		Specification
Electrical (For more complete specifications see Section 3.4)		
Scan Frequency	-	Variable From 20 IR frames/40 Fields per sec to 62 IR frames/124 Fields
Freq. Drift	-	±10% from ambient setting when exposed to environmental conditions
Interlace	-	2:1 or 1:1 interlace depends on wiring on mating connector for the visible collimating optics mounted at either the side or rear.
Scan Direction	-	Adjustable operation for all scan angles up to ±5° for frequencies of 20 to 60 Hz. Direction can be selected to meet system requirements with visible optics mounted at side or rear of Scanner.
Power Supply Requirements		+5.0 ±0.3 VDC (1.0amp peak) 0.65 watts max 0.1 V_{pp} ripple -5.0 ±0.3 VDC (1.0amp peak) 0.25 " " *+15.0 ±0.5 VDC (1.5amp peak) 66 " " 0.2 V_{pp} ripple *-15.0 ±0.5 VDC (1.5amp peak) *For 20-30 Hz operation ±15VDC may be reduced to ±5 VDC Total Power - 4.0 watts max
Rise Time	-	0.5 seconds
Supply Tracking	-	+15 VDC turn on rise times ≤ ±5 VDC supplies ±5 VDC rise times track within 20%
Impedance	-	0.1 ohm to 10 kHz, 5 ohms to 100 kHz
Scan Efficiency	-	70% min for scan angle to 10 degrees scan frequencies 20 to 62 Hz
Mechanical		
Weight	-	0.35 lbs. max.
Dimensions	-	See Figure 3-1.

NOTE

Mechanical specifications involved with interface requirements are included in Section III.

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The Scan and Interlace module processes inputs from a Scanner module scan transducer and interlace transducer to provide drives for the scan mirror motors and interlace solenoids of the Scanner. It also provides an IR Gate pulse to the Auxilliary Control module for blanking and scan failure protection. By strapping the proper mating connector pins, the Scan and Interlace can be made to synchronize the system scan rate to an external signal such as a television vertical sync pulse. Additional strapping is used to select one of 3 possible interlace modes.

The three interlace modes are 2:1 rear, 2:1 side, and 1:1. The terms "rear" and "side" refer to the position of the Visual Collimator module relative to the Scanner module. The phase relationship of the scan mirror position and the interlace position is shifted 180 degrees between these two modes. The term "2:1" refers to the fact that there are 2 interlace positions for each full scan cycle. The 1:1 interlace mode provides one interlace position for one full scan cycle and the second interlace position for the following full scan cycle.

2.2 THEORY OF OPERATION

2.2.1 SCANNING (Refer to Schematic Figure 2-1 and waveforms, Figure 2-2)

The scan drive electronics and the scan mirror form an electromechanical oscillator. The electronics, with feedback information from the scan position transducer, control the waveform and amplitude of this oscillation.

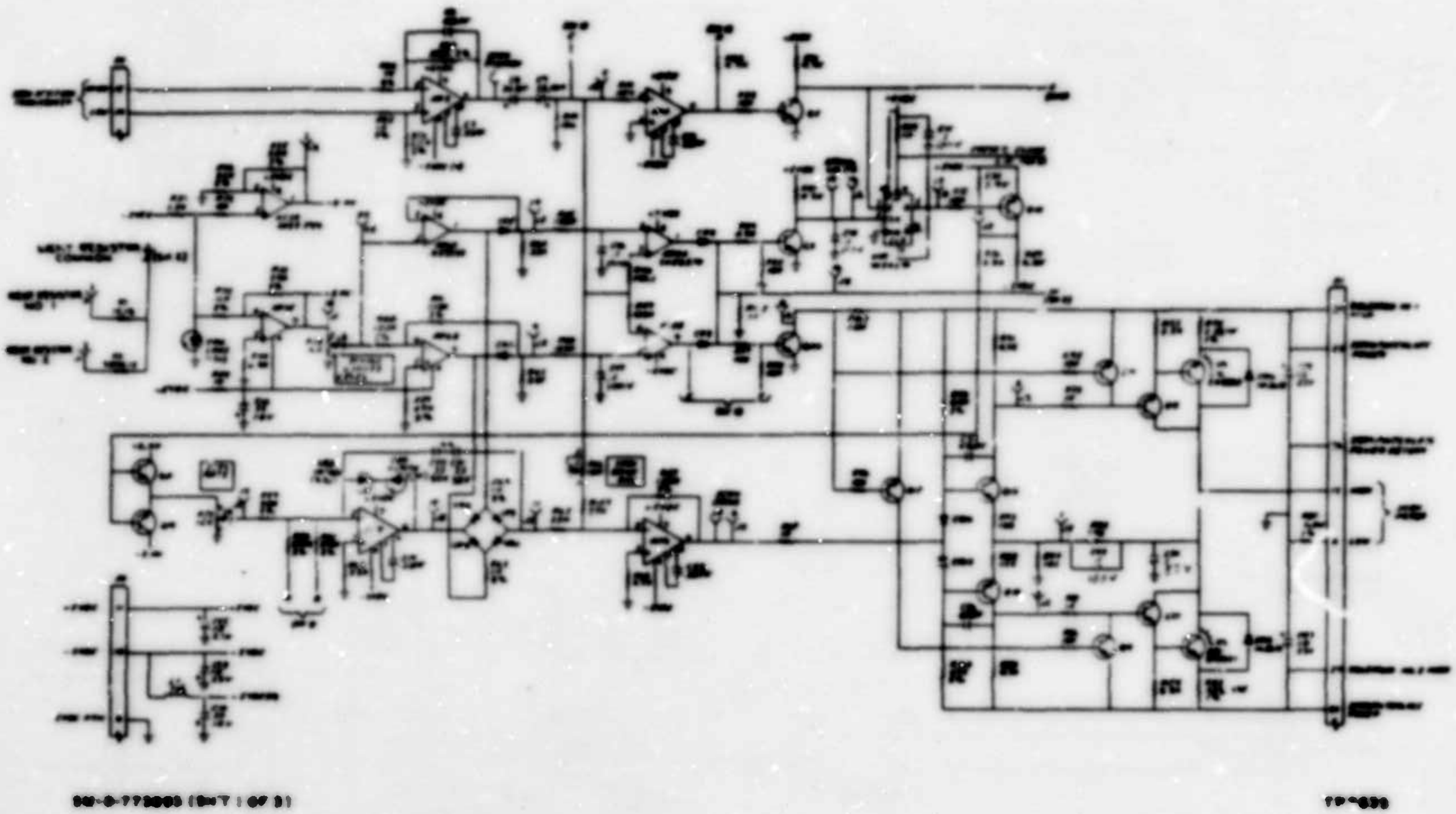
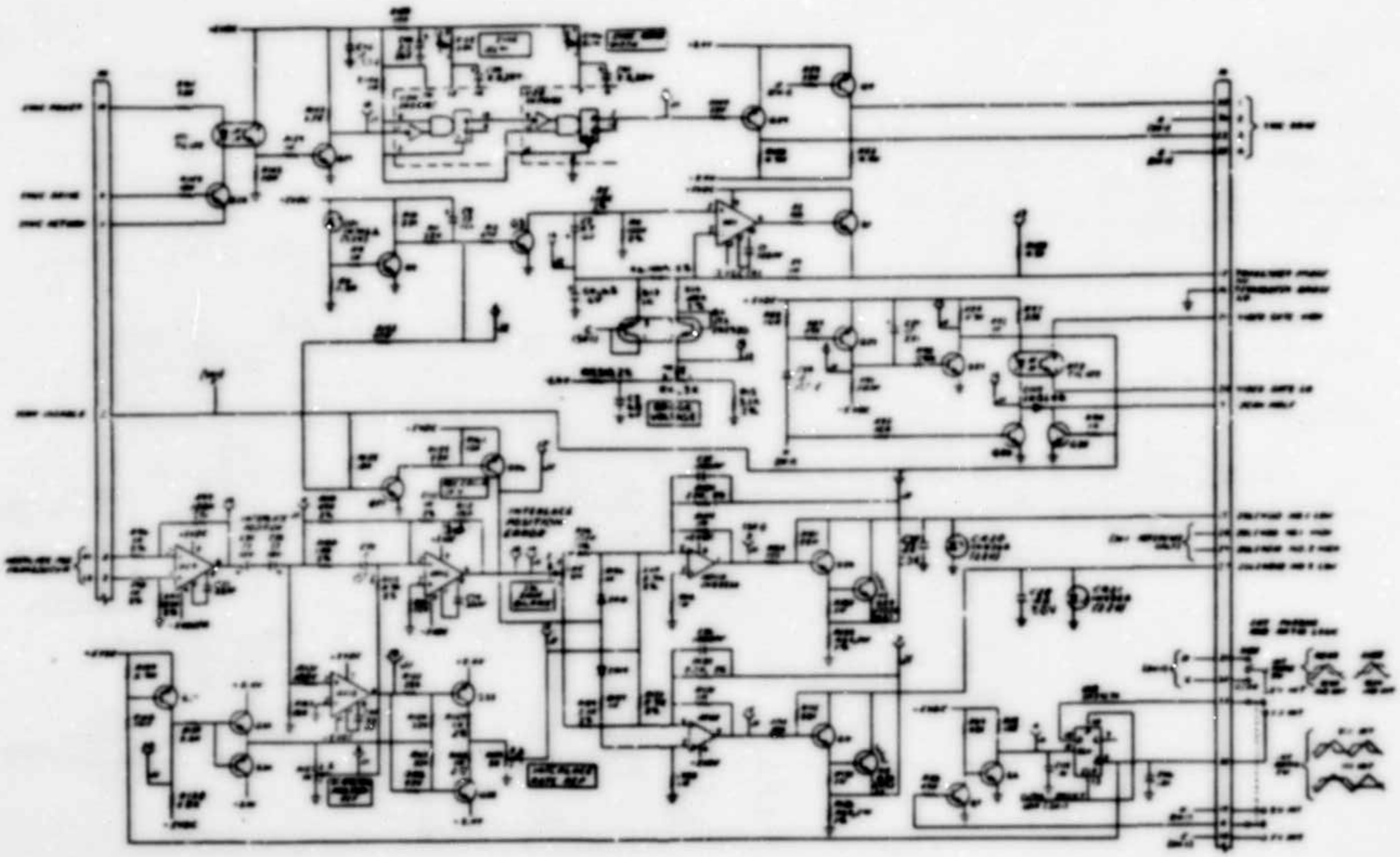


Figure 2-1. Scan and Interlace Module (60 Hz) Schematic Diagram
(Sheet 1 of 2)



TP2636

Figure 2-1. Scan and Interlace Module (60 Hz)
Schematic Diagram (Sheet 2 of 2)

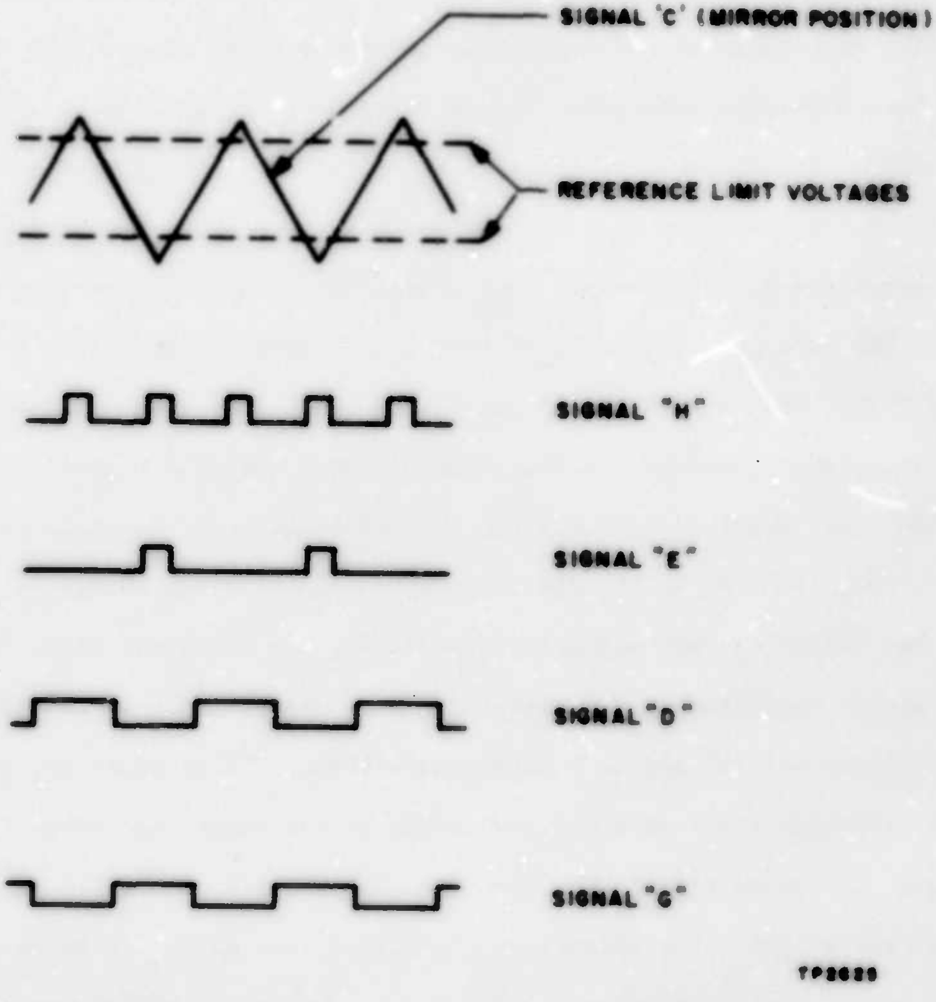


Figure 2-2. Simplified Scan and Interlace Waveforms

The output of the scan position transducer is buffered and amplified by AR2. After AC coupling this signal is labeled signal "C". (Figure 2-2).

U1A is an edge-triggered, type D flip-flop (FF). Q10, Q11, and Q12 buffer the output of U1A and apply it to "scan rate" control (R58). R58 output is integrated and limited by AR7 and a diode bridge (CR9 thru CR12), to form a clipped triangular reference waveform (available on J2-11). This waveform is compared to scan position signal "C", (attenuated by "scan drive Bal" control, R66) in error amplifier, AR8. The error signal (AR8 output) is amplified by Q13 thru Q21 (power amplifier) to drive the scan motor.

Two reference voltages, +2.4VDC and -2.4VDC are generated by CR4, AR3A and AR3B. The +2.4VDC is applied to "spring limits level" control (R38) to generate two reference limit voltages in AR6A and AR6B. AR5A and AR5B form a two level comparitor, comparing the reference limit voltages to signal "C". One limit is in the direction (+ or -) which represents CW rotation of the mirror as represented on signal "C", and the other limit is in the direction representing CCW rotation. When either limit is reached (e.g., when the mirror has rotated to a point where signal "C" is equal to, or greater than, the reference limit voltage) the output of the comparitor (signal "H") goes high. A high on signal "H", thru Q40, Q14 and Q17, shuts off the drive to the scan motors. The inertia of the scan mirror causes it to continue until the bounce springs reverse its direction. Signal "C" decreases in amplitude, tracking the reversed mirror travel. When signal "C" becomes equal to, or less than the reference voltage, signal "H" drops from a high to a low. The change in "H" resets the FF (U1A), reversing the mirror drive voltage polarity, and Q40, Q14 and Q17 shut off, turning the motor drive amplifier back on.

2.2.2 SCAN SYNC

The Scan and Interlace module is capable of operating in sync with an externally generated pulse. The sync circuit squares the sync pulse and the mirror position pulse. The phase difference between the two squared signals is detected and adjusts the scan motor drive to minimize the phase difference.

The input sync signal is isolated by optical coupler FT1. Buffer Q37 drives "sync delay" one shot, U2A, which then drives "sync drive width" one shot U2B. The output of U2B, buffered by Q39 is the squared sync signal (Signal "B", Figure 2-2).

The triangular scan position signal (signal "C") is squared by comparitor AR4. AR4 output is signal "D". "D" is inverted by Q5 to obtain signal "G". "G" is inverted and amplified by Q9 to obtain signal "A".

Signals "A" and "B" are summed integrator AR7. Signal (A + B) is the phase error signal which locks the scan frequency to the input sync frequency. In the absence of a sync input signal, the scanner runs at its own free running frequency determined by R58.

2.2.3 MIRROR POSITION SIGNAL AMPLITUDE

To compensate for drift in the mirror position transducer output amplitude, the transducer bridge voltage is controlled. Signal "C" (mirror position) is fed to diode connected Q4 (pins 1 & 2). This with C4, forms a peak rectifier. The DC voltage, from the peak rectifier, is compared with a DC reference from R16, "bridge voltage" control. Error amplifier AR1 and Q1 drive the transducer bridge to a value which keeps the detected mirror position voltage constant by feedback action.

2.2.4 VIDEO GATE

The Scan and Interlace module generates a video gate pulse which can be used by the video auxilliary module to blank the video display. This pulse

is generated during the mirror turn-around time. Signal "H" (scan limit) drives Q24 which drives photo-coupler AT2. The output of the properly biased AT2 is the video gate pulse.

AC coupling in the video auxilliary module requires pulsing on the video gate signal to keep the display on. Therefore, if the video gate signal is on continuously, the display will be shut off. If scan is lost, Q22 stops pulsing, allowing Q23 to turn off, which turns Q25 on. When Q25 is on, AT2 is on full time, keeping the video gate signal on and blanking the display.

2.2.5 INTERLACE SERVO

For interlace the scan mirror is tilted by solenoids 1 and 2 rotating the scan mirror gimbal. The interlace position transducer output is sensed by amplifier AR4. An "interlace position" reference voltage is developed across R151 ("interlace position REF" control). These two signals are applied to error amplifier AR10. AR10 output drives the two solenoid driver amplifiers, AR11A and AR11B. Solenoid #1 is driven from "+" to ground thru NPN transistors, Q28 and Q29. Solenoid #2 is driven from "-" to ground thru PNP transistors, Q30 and Q31. Thus they are effectively in class "B" and are never on together. AR12, Q32 and Q33 generate a reference voltage to R134, "interlace rate REF" control. R134 output is summed into AR11A and AR11B inputs, controlling the peak drive to the solenoids affecting the time required to switch from one interlace position to the other.

Two interlace phase relationships are possible, 2:1 and 1:1. The 2:1 interlace gives two interlace positions for each scan cycle (scan one direction for 1 interlace position and return scan on 2nd interlace position). The 1:1 interlace gives one complete scan cycle per interlace position.

The interlace phase is selected by a switch, or by jumper connections, thru P1. These determine the inputs to "D" and "clock" connections of U18, a "D" type-triggered flip-flop (FF). For 1:1 interlace U18 is connected as a divide-by-2 circuit clocked by signal "E". Signal "E" pulses only for one complete scan cycle. The output state of U18 sets the polarity of solenoid drive thru Q34, Q35 and Q36. Thus the interlace position is switched once per scan cycle.

For 2:1 interlace, the clock input is connected to signal "H", reversing the polarity for each turn around (Ref Fig. 2-2). This yields 2 interlace positions for each complete scan cycle. In the 2:1 interlace mode, the interlace position, with respect to scan direction, can be reversed to accommodate the LED mounting. If the LED module is mounted on the rear of the scan module the interlace position relationship must be the inverse of the relationship required when the LED module is mounted on the side of the module. To accommodate this, either signal "D" or its inverse signal "G", is connected to the "D" input of the FF (U18). This results in the interlace being in CW mirror rotation.

2.2.6 SCAN DISABLE

When a positive potential is applied to the scan disable input, the scan motor drive amplifiers and solenoid drive are disabled and the video gate signal is turned on continuously.

The scan disable signal turns on Q40 which, through Q14 and Q17, disables the scan motor drive. It also turns Q25 on, turning on the video gate signal (ref paragraph 2.2.4). Interlace is disabled by turning Q27 on which applies +5V to AR11A and AR11B inputs disabling both solenoid drive circuits.

SECTION III

INTERFACE

3.1 CONFIGURATION

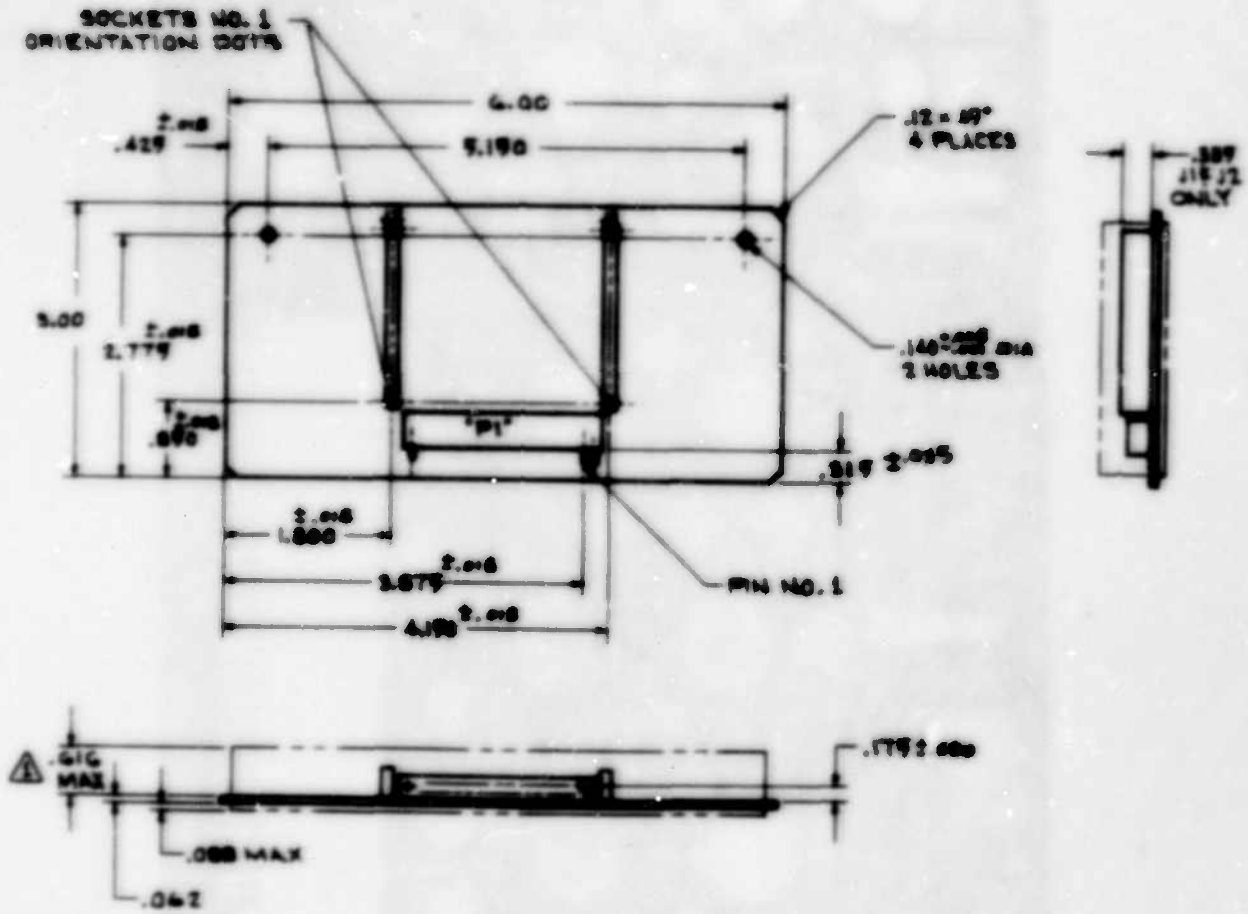
Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating the Scan and Interlace (60 Hz) module in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is a photograph of the module and Figure 3-3 is a parts location drawing.

3.2 INTERCONNECTING

All signals and power connect through P1 to a connector on a mother board or wiring harness. Although the test connectors J1 and J2 are not used in normal operation, the designer should consider providing clearance so that test plugs can be connected without need for an extender on P1. Access should be provided to the test jacks J3 through J8 and for the ten trim poteniometers at the top of the module. Each end of the module must be supported by a suitable mounting slide. For applications involving severe shock or vibration, positive means should be provided to retain the module in the fully engaged position.

3.3 THERMAL DESIGN CONSIDERATIONS

Although the Scan and Interlace (60 Hz) module power dissipation is relatively low (3 watts), it must be taken into account during system design. Refer to Section III fo Chpater I for a detailed discussion of the system thermal design considerations.



NOTES:

1. B2-28A050120 SPEC DENOTES THIS DIM. AS .56 MAX

<u>Tolerances:</u>

.xx = ±.02

.xxx = ±.010

Figure 3-1 Scan and Interlace (60 Hz) Module Outline Drawing

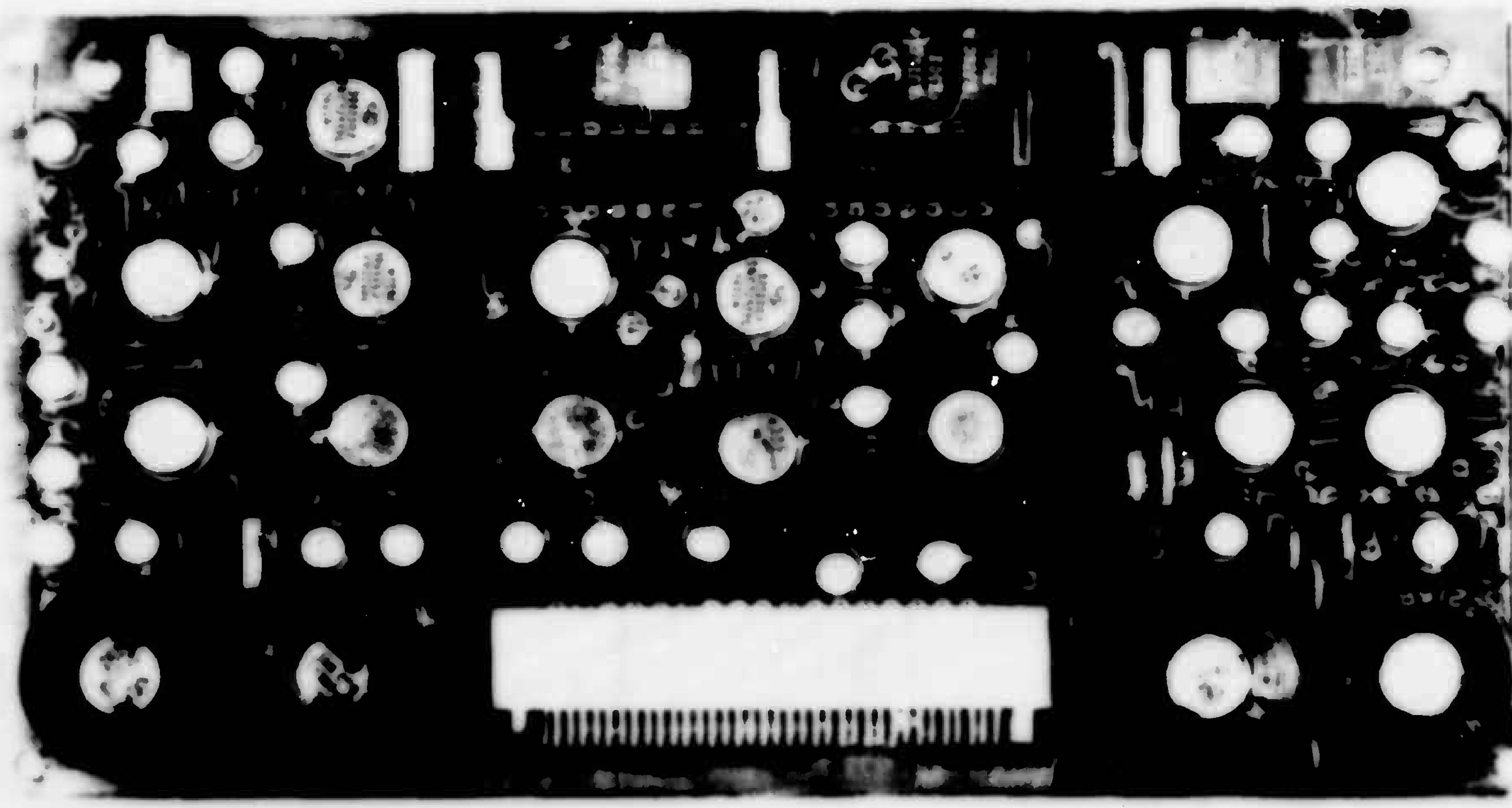


Figure 3-2. Photograph Scan and Interlace Module (60 Hz)

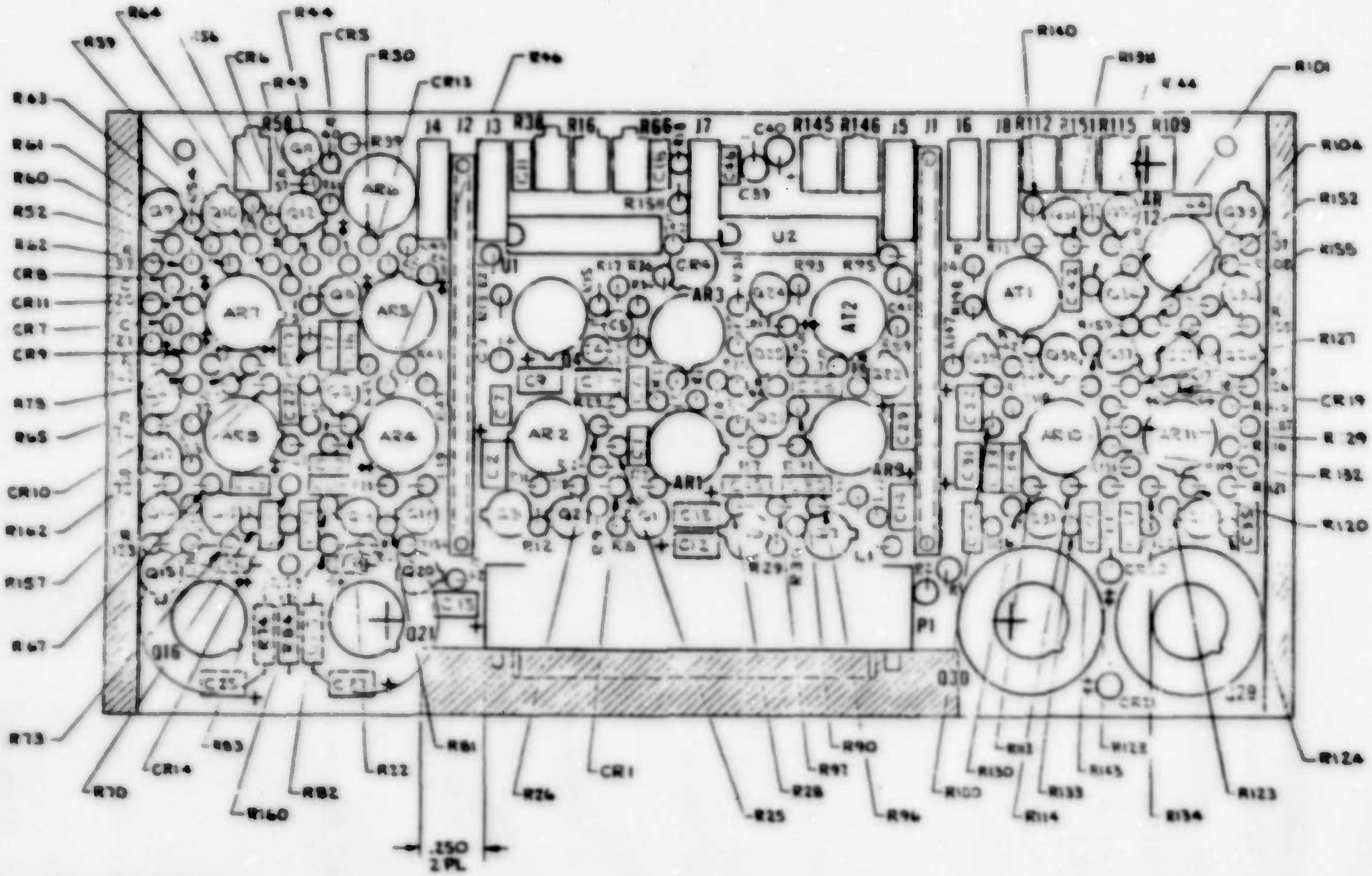


Figure 3-3. Scan and Interlace Module (60 Hz) Parts Location Drawing

3.4 ELECTRICAL INTERFACE DATA

3.4.1 INPUT CHARACTERISTICS (60 Hz High Power)

(a) Voltage/Current/Power:

Voltage	Current	Power
+5.0 ±0.3 volts dc	1.0 ampere peak	0.65 watts maximum
-5.0 +0.3 " "	1.0 " "	0.25 " "
+15.0 ±.05 " "	1.5 " "	6.6 " "
-15.0 ±0.5 " "	1.5 " "	6.6 " "

NOTE:

For 20-30 Hz operation, ±15 Vdc may be reduced to ±5 Vdc and total power required will be 4.0 watts maximum

(b) Ripple: 0.1 volt peak-to-peak maximum on +5 and -5 Vdc
0.2 volt peak-to-peak maximum on +15 and -15 Vdc

(c) Supply rise time: 0.5 second maximum

(d) Supply tracking: +15 and -15 Vdc turn on rise times ≤ the +5 and-5 Vdc rise times; +5 and -5 Vdc rise times shall track within 20%

(e) Impedance: ≤ 0.1 ohm to 10 kHz
≤ 5 ohms to 100 kHz

3.4.2 OUTPUT CHARACTERISTICS

(a) Scan frequency: variable from 20 infrared (IR) frames/40 fields per second to 62 IR frames/124 fields per second; drift ≤ ±10% from ambient setting when exposed to specified static-climatic environments

(b) Interlace: appropriate electrical signals provided to cause scanner mirror to interlace at ends of active azimuth scan travel; adjustable in time domain to permit operation at all scan angles ± 5°; for scan frequencies between 20 and 62 Hz, interlace can be adjusted to provide an interlace signal either once per azimuth scan or once every other azimuth scan

(c) Scan direction: appropriate electrical signals permit operation at 2:1 and 1:1 interlace and for the visible collimating optics

(d) Video gate: video gate output provides an isolated current sink during each scan mirror turn-around; current sink capability = 2.0 milliamperes maximum

(e) Test points: provided to permit set up and checkout of electrical signals which drive and control scan mechanism functions

3.4.3 PROCESSING CHARACTERISTICS

(a) Scan efficiency: 70% minimum for scan angles up to 10° and for scan frequencies of 20 to 62 Hz

(b) Scan jitter in azimuth: 0.75 milliradian maximum in scan mechanism for scan angles up to 10° and scan frequencies between 20 and 62 Hz

(c) Scan jitter in interlace: interlace repeatable with a ±10% deviation of the height of a display element over central 80% of active azimuth scan; maximum change in average interlace movement ±15% of initial setup at +23°C over specified operating temperature range; after soaking at -62°C, interlace will return to within ±15% of initial setup when stabilized at -30°C

(d) Scan failure circuit: scan failure circuit provided to disable power amplifiers to both scan motors and interlace drivers should scan mirror stop

3.4.4 ANCILLARY ELECTRICAL DESIGN CONSIDERATIONS

(1) To assist in the understanding of the interrelationship among the electrical, electromechanical and mechanical operations of the Scan and Interlace module, a block diagram is provided (see Figure 3.4.1)

(2) Information relative to Scan and Interlace Drive Waveforms, Scan Position Amplitude as a Function of Scan Angle, and Spring Limit Width will be found in Figures 3.4-2 through 3.4-4 respectively. Descriptions and information concerning Test Jack Designations (including measured values and other information available at the test jacks), Variable Resistor Adjustments, Optical Circuit Functions, Circuit Descriptions, Formula for Determining Angle between Spring Stops, and Polarities of Transducers, Solenoids and Torquers will be found in Tables 3.4-1 through 3.4-6 respectively.

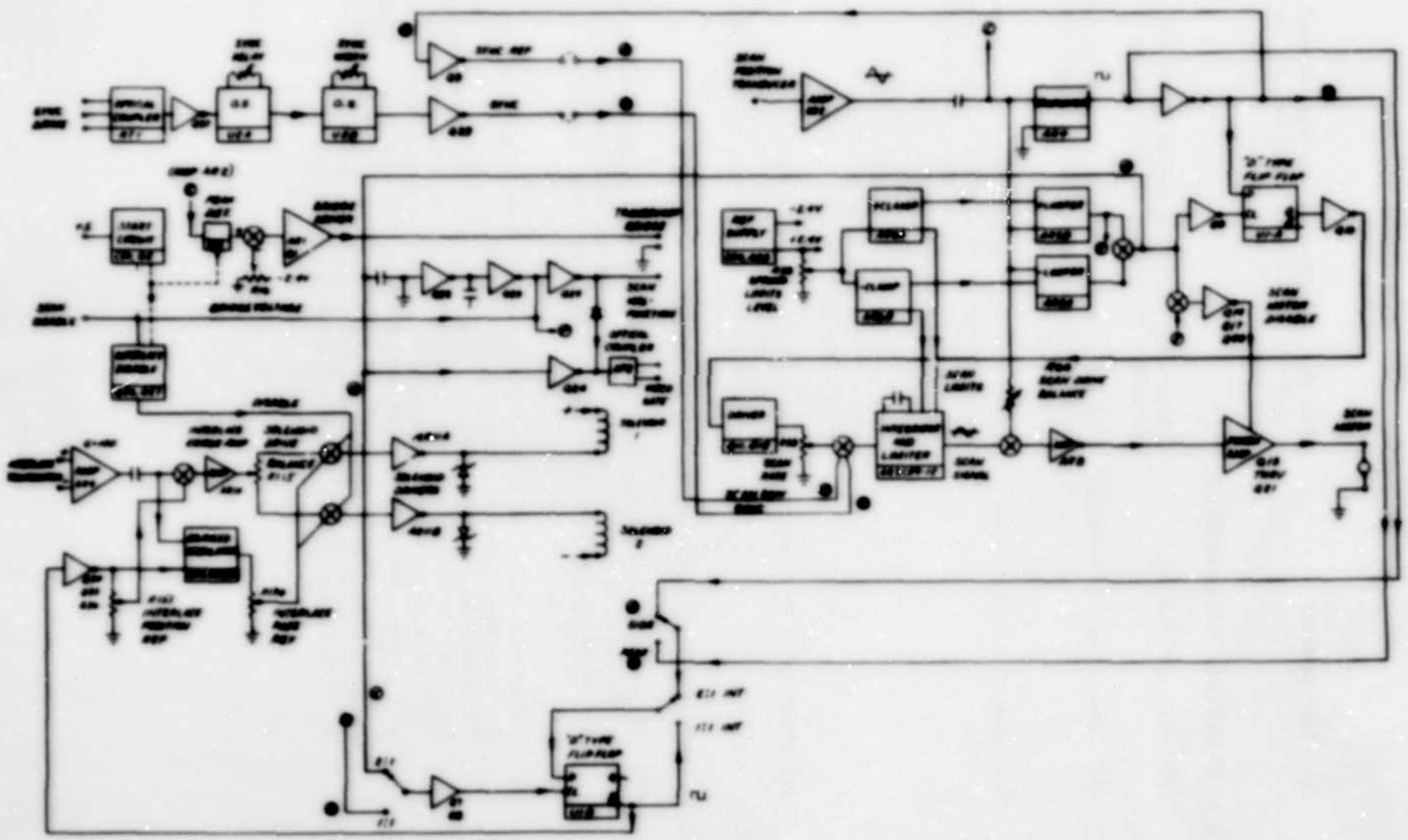
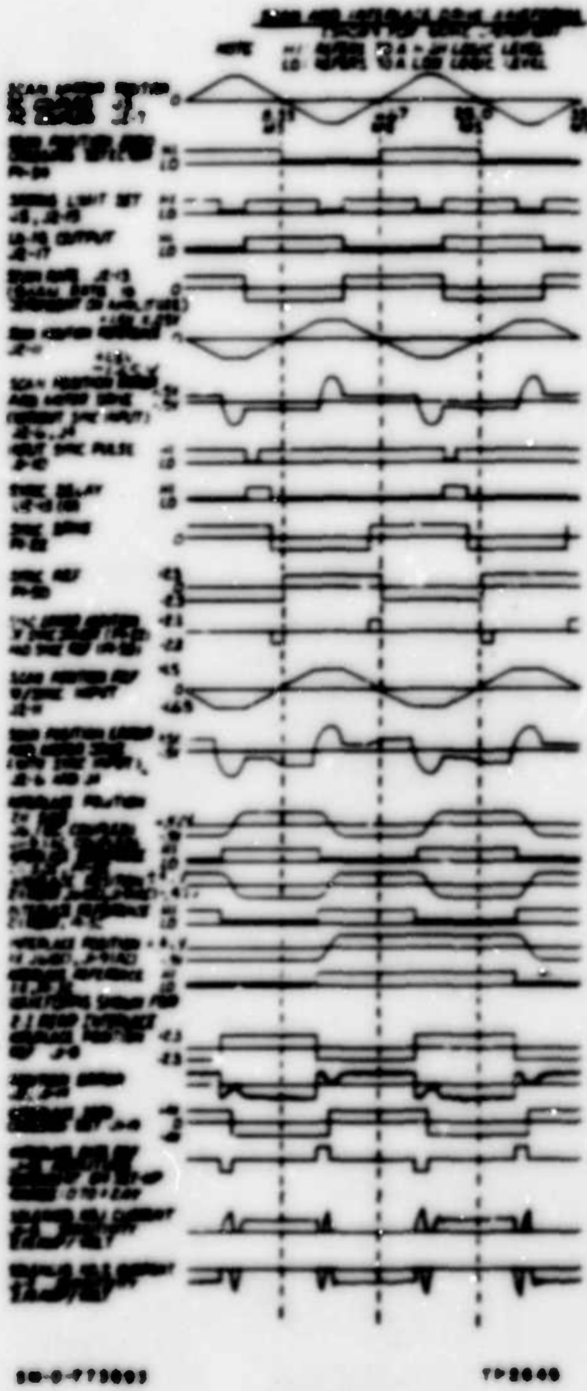


Figure 3.4-1. Block Diagram



Note: 1. Waveforms shown are for 60 Hertz operation.
2. "HI" refers to a high logic level; "Lo" to a low

Figure 3.4-2. Scan and Interlace Drive Waveforms

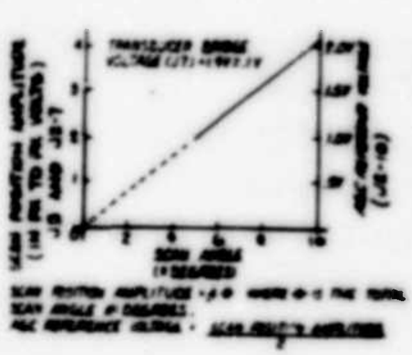


Figure 3.4-3. Scan Position Amplitude as a Function of Scan Angle

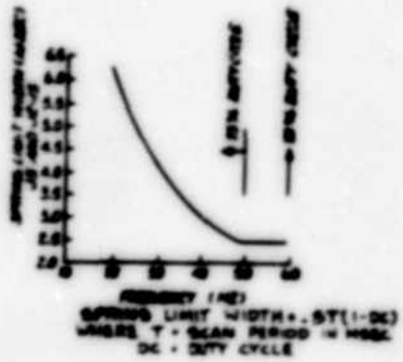


Figure 3.4-4. Spring Limit Width

[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

Table 3.4-1. Test Jack Designation

[illegible]

Table 3.4-2. Variable Resistor Adjustments

[illegible]

Table 3.4-3. Optical Circuit Functions

[illegible]

Table 3.4-4. Circuit Description

[illegible]

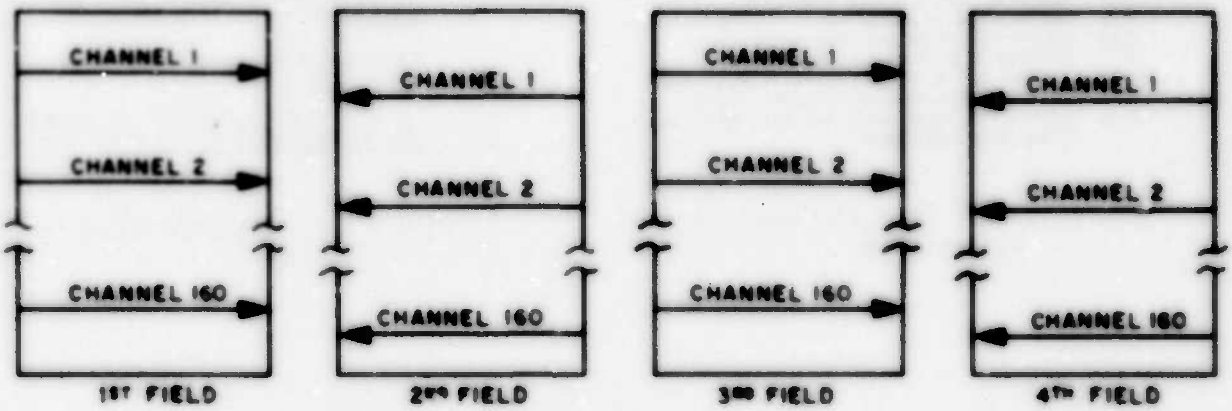
Table 3.4-5. Formula for Determining Angle Between Spring Stops

[illegible]

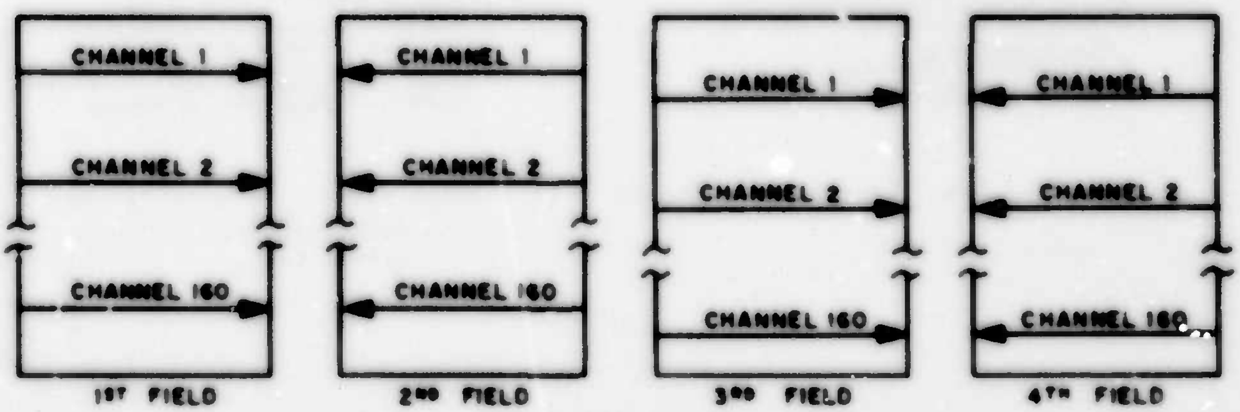
Table 3.4-6. Polarities of Transducers Solenoids and Torquers'

(3) A 2:1 and 1:1 interlace as specified for the Scan and Interlace Module is defined as follows:

<u>2:1 Interlace</u> (Arrow indicates scan line and direction of azimuth scan)



<u>1:1 Interlace</u> (Arrow indicates scan line and direction of azimuth scan)



(4) This Scan and Interlace module (60 Hertz, high power) should be used when the system unique input power is not unduly restrictive, and a scan frequency as low as 20 Hertz or as high as 62 Hertz and a scan angle of up to 10 degrees is required. If the system unique input power is limited and a scan frequency of 30 Hertz and a scan angle of up to 5.5 degrees is acceptable, Scan and Interlace, drawing No. SM-D-773894 (30 Hertz, low power) should be used.

TP2821

3.4.5 INPUT CHARACTERISTICS (30 Hz Low Power)

(a) Voltage: +4.8 and -4.8 volts dc
+10 and -10 volts dc

(b) Power: to operate low-power board and scanner 2.2 watts maximum for active scan angle ≤ 5.5

3.4.6 OUTPUT CHARACTERISTICS

(a) Scan frequency: adjustable to 30 ±0.5 Hz; drift ±3 Hz maximum from ambient setting when exposed to specified static-climatic environments

(b) Interlace: appropriate electrical signals provided to cause scanner mirror to interlace at ends of active azimuth scan travel; interlace can be adjusted to provide an interlace signal once per azimuth scan

(c) Scan direction: bidirectional mode at 2 scans per cycle

3.4.7 PROCESSING CHARACTERISTICS

(a) Scan efficiency: 75% minimum for an active scan angle $\leq 5.5°$

(b) Scan jitter in azimuth: 0.75 milliradian maximum in scan mechanism for scan angles up to 5.5°

(c) Scan jitter in interlace: interlace repeatable with a ±10% deviation of the height of a display element over central 80% of azimuth field of view; maximum change in average interlace displacement ±15% of initial setup at +25°C over specified operating temperatur range after soaking at -62°C, interlace will return to within 15% of initial setup when stabilized at -30°C

3.4.8 ANCILLIARY ELECTRICAL DESIGN CONSIDERATIONS

(1) This Scan and Interlace module (30 Hertz, low power) should be used when the system unique input power is limited, and a scan frequency of 30 Hertz and scan angle of no greater than 5.5 degrees is acceptable. If a scan frequency of from 20 to 62 Hertz and/or a scan angle of at least 10 degrees is required, Scan and Interlace, drawing No. SM-D-773894 (60 Hz, high power) must be used (see 3.4)

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the Scan and Interlace module. Presented herein are the test equipment requirements, test set up, adjustment and alignment techniques.

4.2. TEST EQUIPMENT

The following, or equivalent, test equipment is required to perform the necessary operational tests, alignments, and adjustments on the Scan and Interlace module.

4.2.1 STANDARD TEST EQUIPMENT

Table 4-1, following, presents a listing of equipment which has been found to be adequate for testing of this module.

Table 4-1

STANDARD TEST EQUIPMENT

Equipment	Manufacturer	Model
Power Supply (2)	Hewlett-Packard	6227B
Frequency Counter	Hewlett-Packard	5326A
Oscilloscope	Tektronix	453
Scanner Module	USA Ecom	SM-D-773885
Function Generator	Wavetek	110
Digital Multimeter	Fluke	8000A

4.2.2 SPECIAL TEST SEQUIPMENT

Convenient means of interconnecting the various equipment, controls, and simulators used in testing the Scan and Interlace module may be achieved by fabricating a test set. Such a test set may be fabricated from the information in Figure 4-1.

4.3 SPECIAL TOOLS

No special tools are required to test this module.

4.4 TEST SET UP

Figure 4-2 is a diagram of the typical interconnections used in a test set up.

4.5 CALIBRATION/PREPARATION FOR USE

Operational status of the Scan and Interlace module may be determined by the following tests.

4.5.1 ELECTRICAL TESTS AND ADJUSTMENTS

Perform each test of the following paragraphs in the order presented. Verify a proper response or indication before proceeding to subsequent actions.

4.5.1.1 Equipment Interconnection

4.5.1.1.1 Insure that the following switches and controls are positioned as indicated:

TEST EQUIPMENT

±15 Volt Power Supply, LINE:	OFF
± 5 Volt Power Supply LINE:	OFF
±15 Volt Power Supply, VOLTAGE	Minimum
± 5 Volt Power Supply, VOLTAGE	Minimum
Both Supplies, INDEPENDENT-TRACKING:	TRACKING

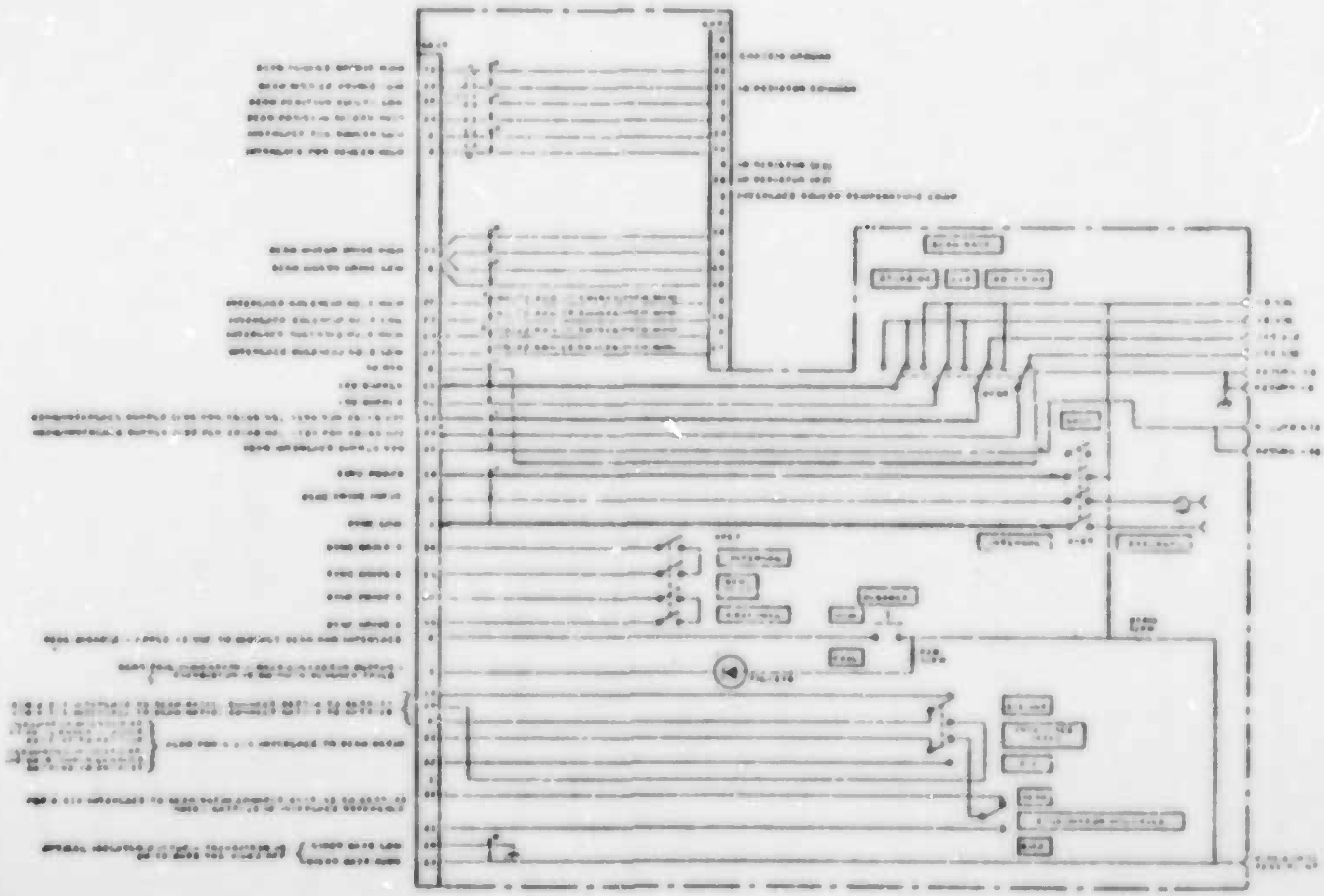


Figure 4-1. Scan and Interface Module Test Set

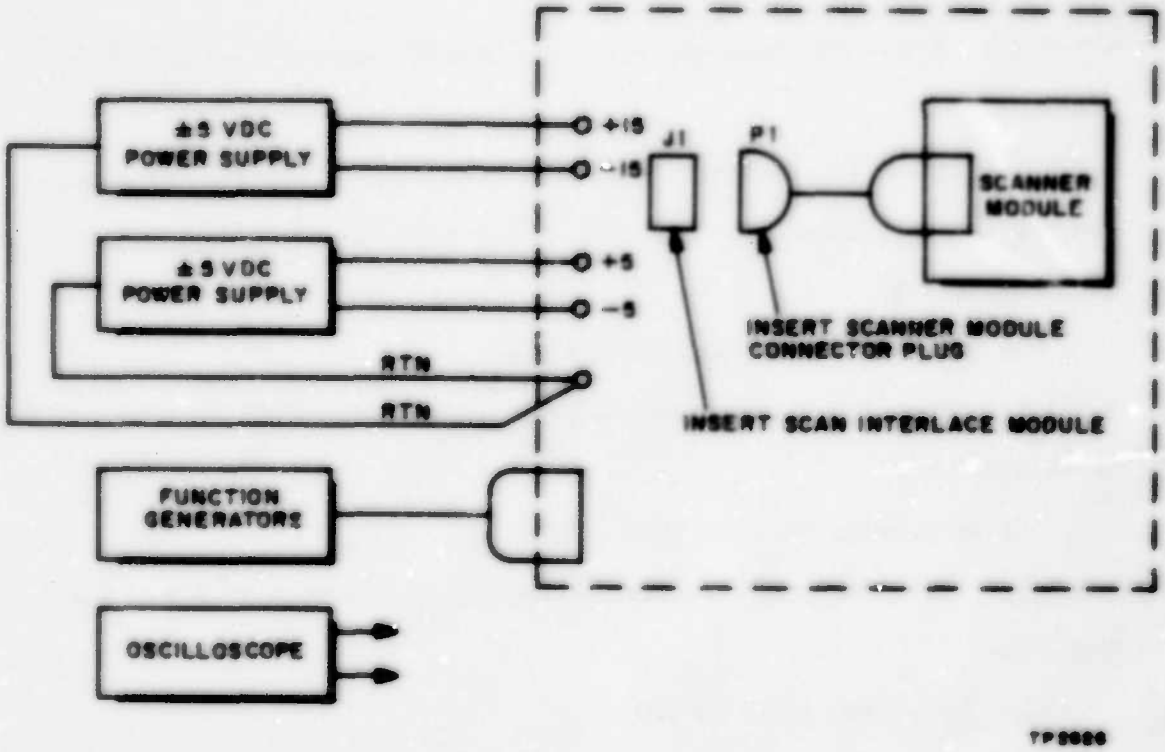


Figure 4-2. Scan and Interlace Module Test Setup

TEST SET

SCAN RATE:	OFF
SYNC:	INTERNAL
SYNC MODE	INTERNAL
INTERLACE RATIO:	2:1
COLLIMATOR MOUNTING:	REAR

4.5.1.1.2 Insert the Scan and terlace Module into test set J1. (See Figure 4-2).

4.5.1.1.3 Using the ohmmeter function of the digital multimeter, measure the resistance between J1-1 and J1-2 on the Scan and Interlace Module. (See Figure 4-3)

The resistance shall be 1000 ±20 ohms.

4.5.1.1.4 Measure the resistance between J1-3 and J1-2 of the Scan and Interlace Module.

The resistance shall be 9090 ±180 ohms.

4.5.1.1.4 Turn the power supplies on and adjust for ±5.0 ±0.3 Vdc and ±15.0 ±0.5 Vdc.

Then turn power supplies off.

4.5.1.1.5 Interconnect all test equipment as shown in Figure 4-2.

4.5.1.1.6 Interconnect scanner module with test set.

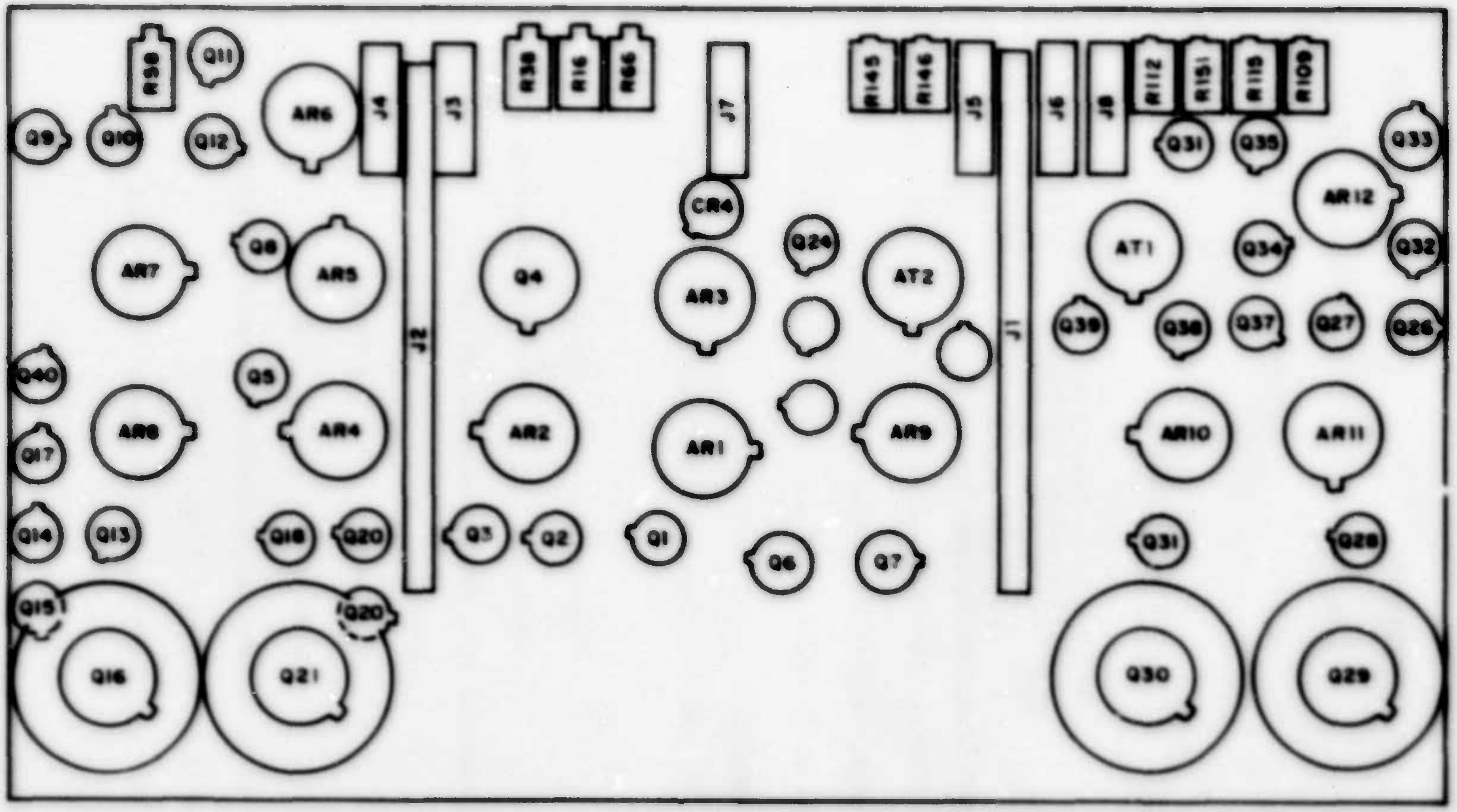
4.5.1.2 <u>Input Current Measurement</u>

4.5.1.2.1 Turn power supplies on.

Set SCAN RATE to 40-60 Hz Position.

4.5.1.2.2 Momenterily depress the DISABLE SWITCH which measuring the current from each of the power supplies.

The current for each of the supplies shall be within the following limits:



TP2030

Figure 4-3 Scan and Interlace Module Control and Test Jack Location Drawing

VOLTAGE	CURRENT	VOLTAGE	CURRENT
+5.0 Vdc	< 130 MA	+15 Vdc	< 440 MA
-5.0 Vdc	< 50 MA	-15 Vdc	< 440 MA

NOTE:

Unless otherwise indicated, the test jacks referred to in subsequent paragraphs are located on the Scan and Interlace Module. See Figure 3.

4.5.1.3 Scan Frequency Without Sync

4.5.1.3.1 With the SCAN RATE switch in the 40-60 Hz position, using a frequency counter, measure the frequency at J3.

The frequency shall be 58 ±1 Hz. Turn SCAN RATE off.

4.5.1.3 Scan Drive

4.5.1.3.1 Set the function generator to provide a triangular wave output as follows:

Frequency:	60 Hz
Amplitude:	4.0 Vdc (positive going)

4.5.1.3.2 Position test set switches as follows:

SYNC:	EXTERNAL
SYNC MODE:	EXTERNAL
SCAN RATE	40-60 Hz

4.5.1.3.3 Using the digital multimeter, measure the voltage at J7.

The voltage shall be 1.9 ±0.1 Vdc.

4.5.1.3.4 Set the oscilloscope to external trigger and sync to the input signal.

Connect oscilloscope channel A to J7.

The 60 Hz component of the ripple shall be no more than 20 mv p-p.

4.5.1.3.5 Move the oscilloscope channel A input to J3.

The displayed waveform shall be similar to Figure 4-4A.

The amplitude shall be 4.0 ±0.2 Vp-p.

DC offset shall be no more than 0.5V.

4.5.1.3.5 Connect oscilloscope channel B to function generator output. Adjust oscilloscope to display one cycle of monitored signal at J3.

Verify that both waveforms displayed by oscilloscope channels A and B are stable.

4.5.1.3.6 Connect oscilloscope channel A to J4.

The waveform displayed shall be similar to figure 4-4D. Sync error ramp times should be approximately equal.

4.5.1.3.7 Connect oscilloscope channel A to J5.

The displayed pulse train, (see Figure 4-4E) shall have the following characteristics.

Frequency:	120 Hz
Width:	2.2 ±2.5 msec
Amplitude	4 Vp-p

4.5.1.4 Interlace Drive

4.5.1.4.1 Connect Channel B of the oscilloscope to J6.

The scan position signal displayed should be similar to Figure 4-4A. The average amplitude should be 0.84 ±0.06 Vp-p.

4.5.1.4.2 Connect Channel A of the oscilloscope to J3.

The trapezoidal waveform (interlace position) displayed on Channel A and the triangular waveform on Channel B should be similar to and have a phase relationship as shown in Figure 4-4A.

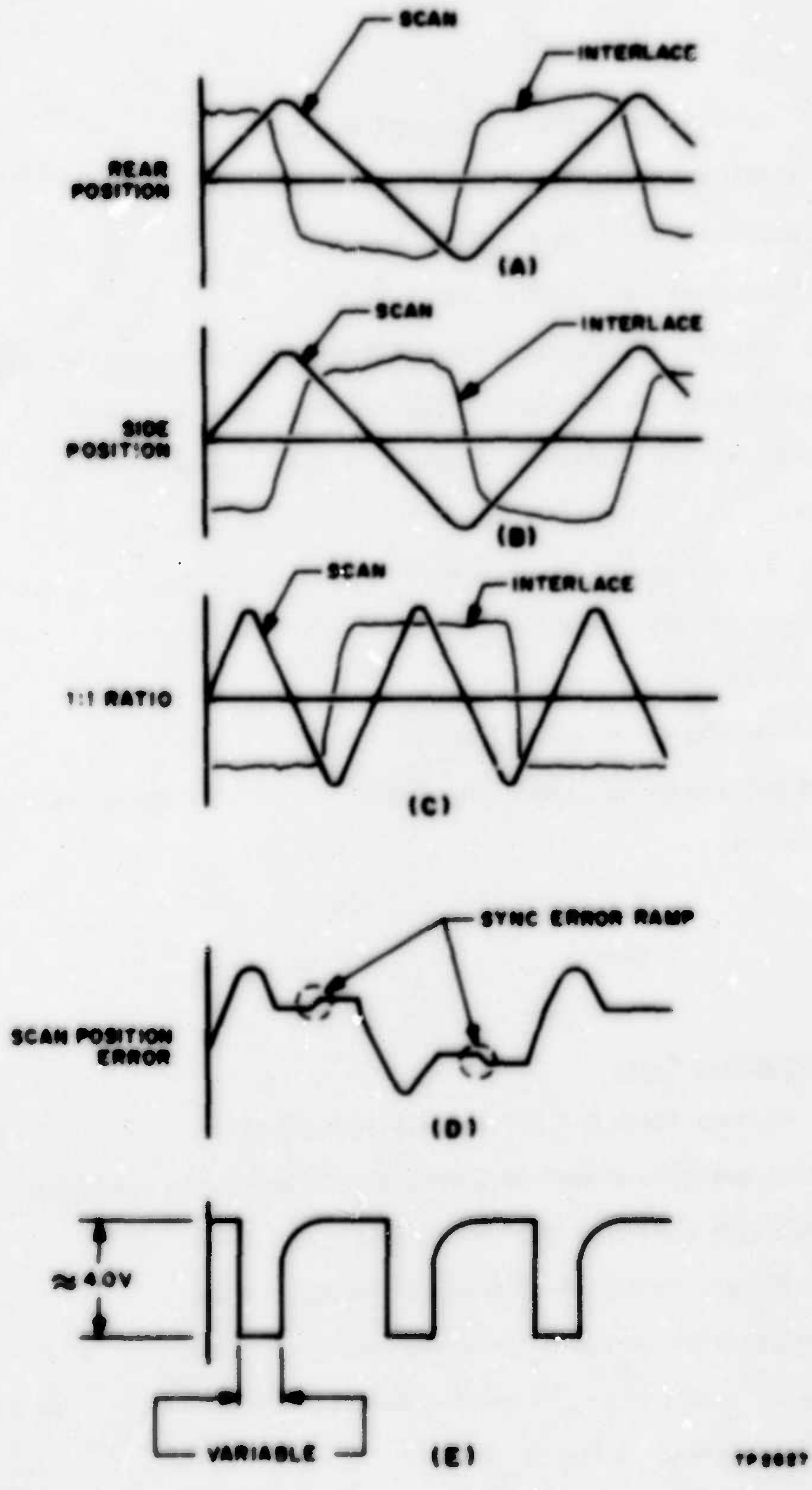


Figure 4-4 Scan and Interlace Waveforms

4.5.1.4.3 Set the COLLIMATOR MOUNTING switch on the test set to side position.

The waveform displayed on oscilloscope Channel A shall shift 180° from that observed in paragraph 4.5.1.4.2. See Figure 4-4B.

4.5.1.4.4 Position the test set INTERLACE switch to 1:1

The frequency of the displayed waveform on Channel A shall be reduced to one half that of paragraph 4.5.1.4.3. See Figure 4-4C.

4.5.1.4.5 Return INTERLACE switch to 2:1 and COLLIMATOR MOUNTING switch to REAR; SCAN RATE to off.

4.5.1.4.6 Depress SCAN DISABLE and set SCAN RATE to 40-60 Hz.

Scanner shall not start. Release SCAN DISABLE

Scanner shall not start.

4.5.1.4.7 Set SCAN RATE to OFF for approximately 3 seconds, then return to 40-60 Hz.

Scanner shall start.

4.5.2 MECHANICAL ALIGNMENT

The Scan and Interlace Module requires no mechanical alignment upon installation in a system other than to provide for access to the ten adjustment potentiometers.

4.5.3 ADJUSTMENT IN THE SYSTEM

Scan and Interlace Module adjustments within the system will consist of refining the potentiometer settings to compensate for minor System and Scanner module characteristics variations normally encountered during fabrication. With the system operating, perform the following.

4.5.3.1 Connect an oscilloscope to J5. Adjust R38 for a pulse width of 2.5 ±.25 msec.

4.5.3.2 Connect the oscilloscope to J2-13. Adjust R58 to set the square wave amplitude to 2.0 ±0.2 Vp-p.

4.5.3.2 Connect oscilloscope Channel A to J1-10 and Channel B to J1-12. Adjust R145 for a 2.1 msec delay from negative going edge on Channel A to positive going edge on Channel B. Adjust R146 for an approximate square wave at J1-12.

4.5.3.3 Connect oscilloscope Channel A to J4. Adjust R66 and R58 to provide an output waveform as shown in Figure 4-4D.

4.5.3.4 Connect oscilloscope Channel A to J6; verify waveform to be 0.84 ±.06 Vp-p.

4.5.3.5 Connect oscilloscope Channel B to J1-8. Adjust R151 for a signal level of approximately 2 volts p-p.

4.5.3.6 Connect oscilloscope to J1-13. Adjust R109 for an output of 0.5 ±.05 volts p-p.

4.5.3.7 Connect the oscilloscope to J8. Adjust R112 and R151 for a waveform as shown in Figure 4-5A.

4.5.3.8 Connect oscilloscope Channel A to J1-5 and channel B to J1-7. Adjust R115 to provide equal amplitudes of the displayed signals. See Figure 4-5B.

4.5.3.9 Connect a digital voltmeter to J-7. Adjust R16 for 1.9 ±.1Vdc.

4.6 SPECIAL MAINTENANCE

The Scan and Interlace Module requires no special maintenance attention beyond the routine procedures followed for general electronic equipment. No time change components are contained in this module.

4.5.3.2 Connect oscilloscope Channel A to J1-10 and Channel B to J1-12. Adjust R145 for a 2.1 msec delay from negative going edge on Channel A to positive going edge on Channel B. Adjust R146 for an approximate square wave at J1-12.

4.5.3.3 Connect oscilloscope Channel A to J4. Adjust R66 and R58 to provide an output waveform as shown in Figure 4-40.

4.5.3.4 Connect oscilloscope Channel A to J6; verify waveform to be 0.84 ±.06 Vp-p.

4.5.3.5 Connect oscilloscope Channel B to J1-8. Adjust R151 for a signal level of approximately 2 volts p-p.

4.5.3.6 Connect oscilloscope to J1-13. Adjust R109 for an output of 0.5 ±.05 volts p-p.

4.5.3.7 Connect the oscilloscope to J8. Adjust R112 and R151 for a waveform as shown in Figure 4-5A.

4.5.3.8 Connect oscilloscope Channel A to J1-5 and channel B to J1-7. Adjust R115 to provide equal amplitudes of the displayed signals. See Figure 4-5B.

4.5.3.9 Connect a digital voltmeter to J-7. Adjust R16 for 1.9 ±.1Vdc.

4.6 SPECIAL MAINTENANCE

The Scan and Interlace Module requires no special maintenance attention beyond the routine procedures followed for general electronic equipment. No time change components are contained in this module.

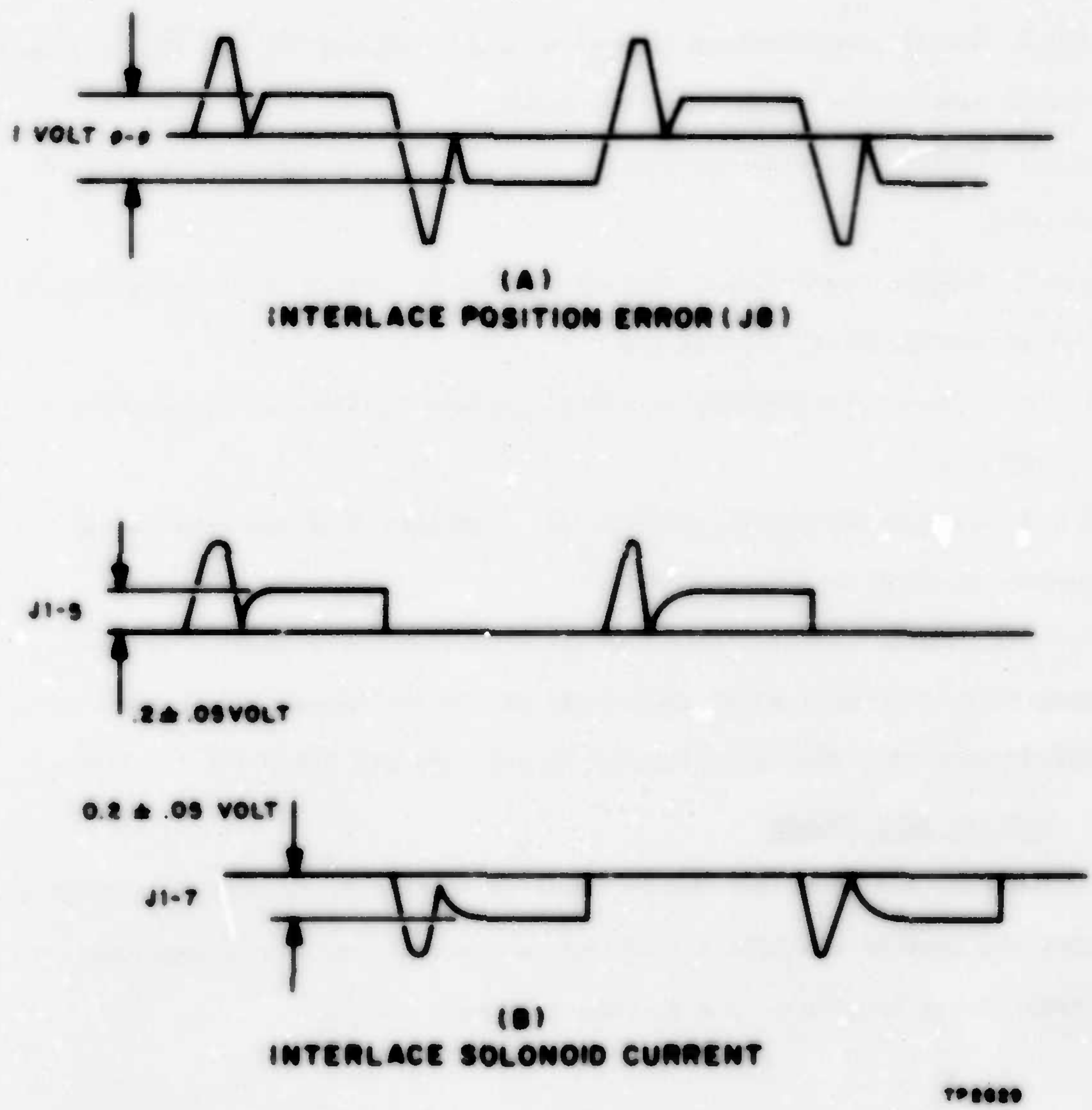


Figure 4-5 Interlace Drive Waveforms

CHAPTER 9

COLLIMATOR, VISUAL, INFRARED
USAECOM SM-D-773397

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Collimator, Visual, Infrared module hereinafter called the visible collimator consists of optical elements which collimate the visible light output from the light emitting diode (LED) array and direct the collimated light onto the back side of the scan mirror of the Mechanical IR Scanner module.

1.2 INTENDED USE OF ITEM

The Visible Collimator module has been designed to be interfaced with other major common or special modules to form a Forward Looking Infrared (FLIR) or Thermal Imaging System. The Visible Collimator is optically interfaced between the Mechanical IR Scanner and LED Array modules. The function of the Visible Collimator is to receive the visible light emitted by the diode elements of the LED array, turn the light 90°, and direct the collimated visible light onto the back side of the scan mirror.

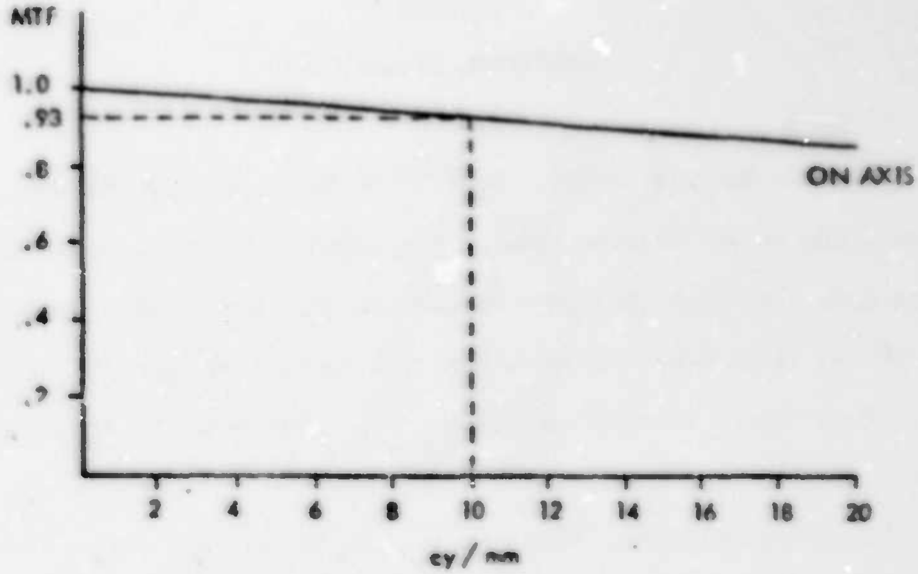
1.3 TECHNICAL SPECIFICATIONS

The technical specifications of the Visible Collimator module are as follows:

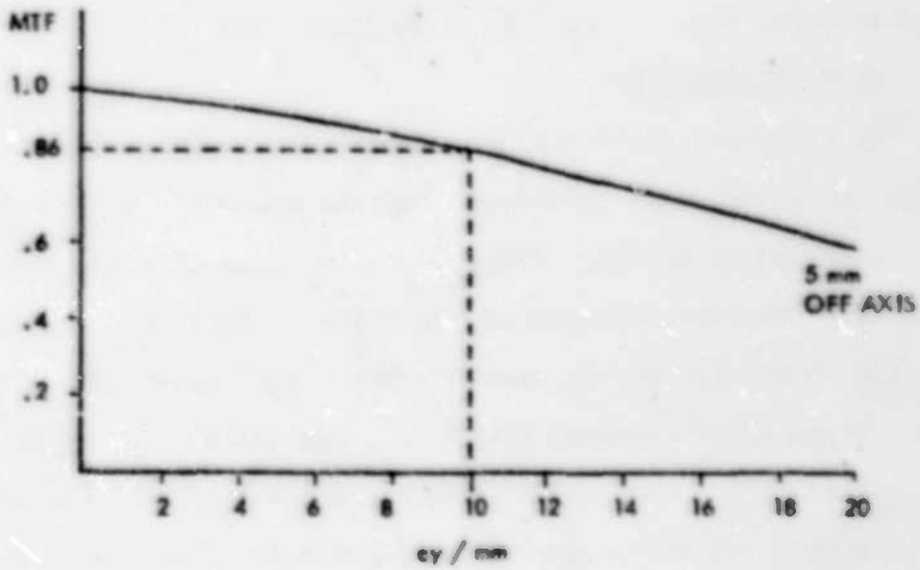
Parameter	Specifications
Effective Focal Length (EFL)	67.8±0.7 millimeters (measured in red light in range of 6300 to 6900 Angstrom units)
F/Number	Faster than f/2.2
Flange Focal Distance (FD)	
(a) With LED field flattener properly positioned in path	11.91 ± 0.25 millimeters
(b) Nominal in air w/o flattener	11.21 millimeters
Field of View (FOV)	Fills circular format diameter of 20 millimeters
Modulation Transfer Function (MTF)	See Figure 1-1
Linear Distortion	Between 4% pincushion and 4% barrel
Relative Illumination	> 60% at edge of field
Stray Light Veiling Glare	< 5%
Optical Transmittance	> 85% in the 6300 to 6900 Angstrom region
Deviation	90° ± 0.5° (degrees)

NOTE

For interface information and as mechanical configuration, outline dimensions and mounting information, refer to Section III.



A



B

Figure 1-1. Visible Collimator MTF ON-Axis and 5mm OFF-Axis

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

In order for the visible light image formed by the LED array to be transmitted by the reverse side of the scanning mirror without distortion, it is necessary that the image be collimated. The Visible Collimator operates at the LED visible wavelength and uses a turning mirror to turn the image 90° and collimate it onto the scan mirror. The lens system has a fixed focus.

As the collimated light energy leaves the Visible Collimator and enters the Mechanical IR Scanner module, it passes through the phase shift lens nullifier and phase shift lens. This lens pair has equal and opposite powers so its effect is essentially that of a flat plate and the LED light is essentially parallel again as it strikes the scan mirror.

2.2 THEORY OF OPERATION

The visual collimator collects light from the LED array and collimates it for the visual scan. Collimated light is preferable for scanning rather than convergent or divergent light, since the focal shifts in the image plane are minimized. The characterstics of the lens which must be considered from a systems standpoint are the same as those enumerated for the IR imager; ie, focal length, clear aperture, distortion, transmission and field of view, and resolution or MTF. When operating in the infrared in the 18-12 micron band, it was pointed out in the numerical example given in Section 1, that diffraction limited performance would be achieved. Since the diffraction limit is a measure of angular resolution directly proportioned to wavelength, a comparison of the diffraction limit for the visible IR is

$\frac{\lambda_{vis}}{\lambda_{IR}} = \frac{.63 \text{ microns}}{10 \text{ microns}} = .063$. Thus a diffraction limited spot size for

the visible is approximately 6% of the diffraction limited spot size for the IR. Since the scene resolution is limited by the infrared scanner portion of the system, the MTF requirements for the visual collimator are not excessive. For example, the IR imager M T F cutoff is approximately 55 line pairs per millimeter at f/1.8, which is not a high visible light diffraction limit. However, in the overall system MTF which is a function of many system parameters, care should be taken in specifying the visual collimator that it does not limit the overall error budget.

SECTION III

INTERFACE

3.1 CONFIGURATION

Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating this module in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is a photograph of the module.

3.2 INTERCONNECTING

The Visible Collimator normally interfaces with the Mechanical IR Scanner and the Light Emitting Diode (LED) Array. It can be operated in any attitude, but must be oriented relative to the mating modules so as to provide the required output image orientation. Angular scales are provided adjacent to both mounting faces to aid in installing modules in the desired positions.

Servo type clamps are used to secure the Visible Collimator to the Scanner and to the LED array. However, because of the relatively weak structure of the Scanner, the Collimator and LED array should have additional support so that their weights do not distort the Scanner structure. Even a small distortion of the Scanner can seriously effect its scan rate.

A special adapter-spacer may be needed between the Visible Collimator and the Scanner. Without such an adapter-spacer, the end of the collimator may extend a maximum of .411 inch into the Scanner, measured from the outside surface. If the Collimator is mounted on the side of the Scanner, there may be interference with the scan mirror. If the Collimator is mounted at the rear of the Scanner, there may be interference with the phase shift lens or the ring mounting it in the gimbal (if such a lens is required in the system).

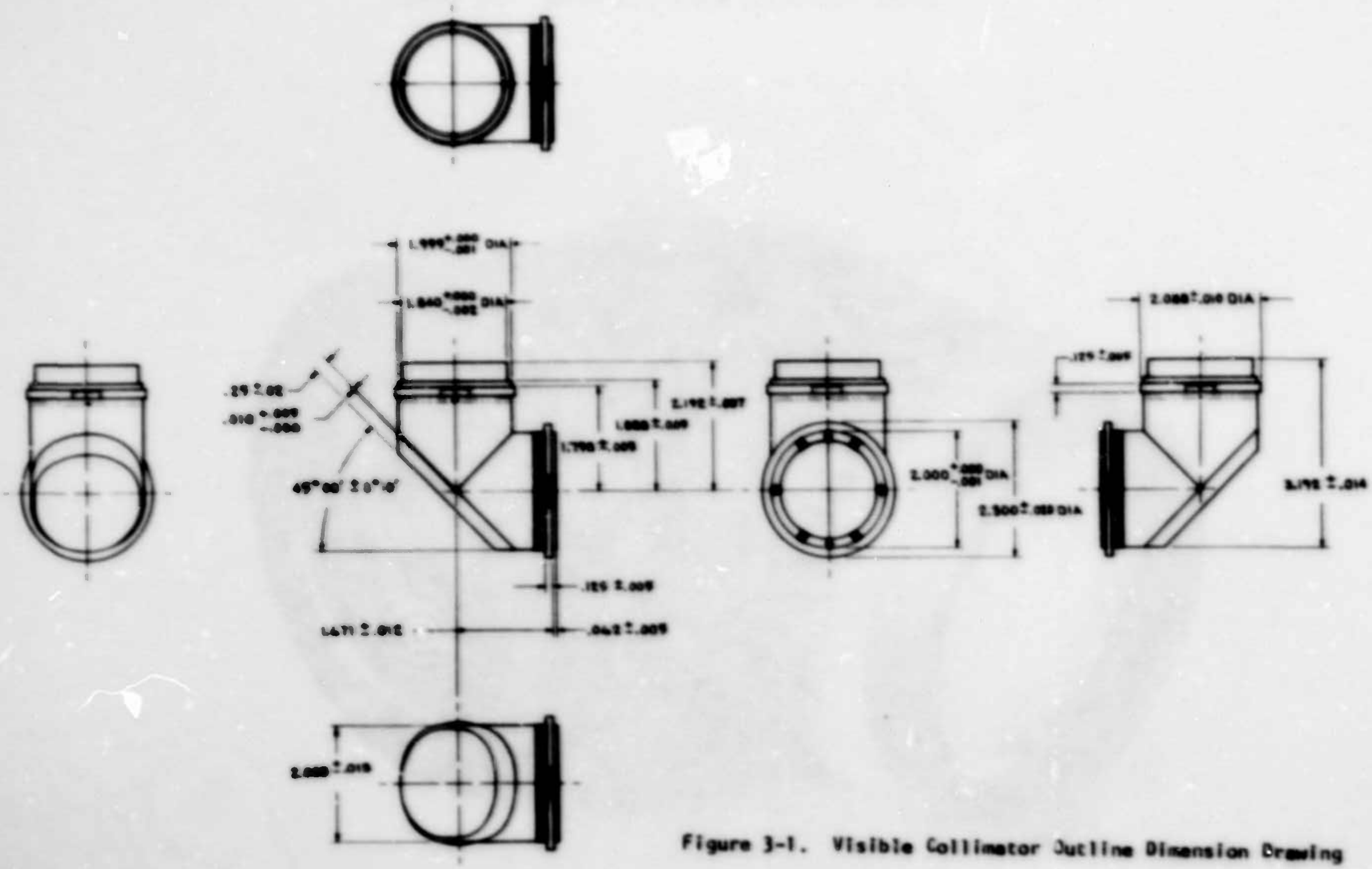


Figure 3-1. Visible Collimator Outline Dimension Drawing

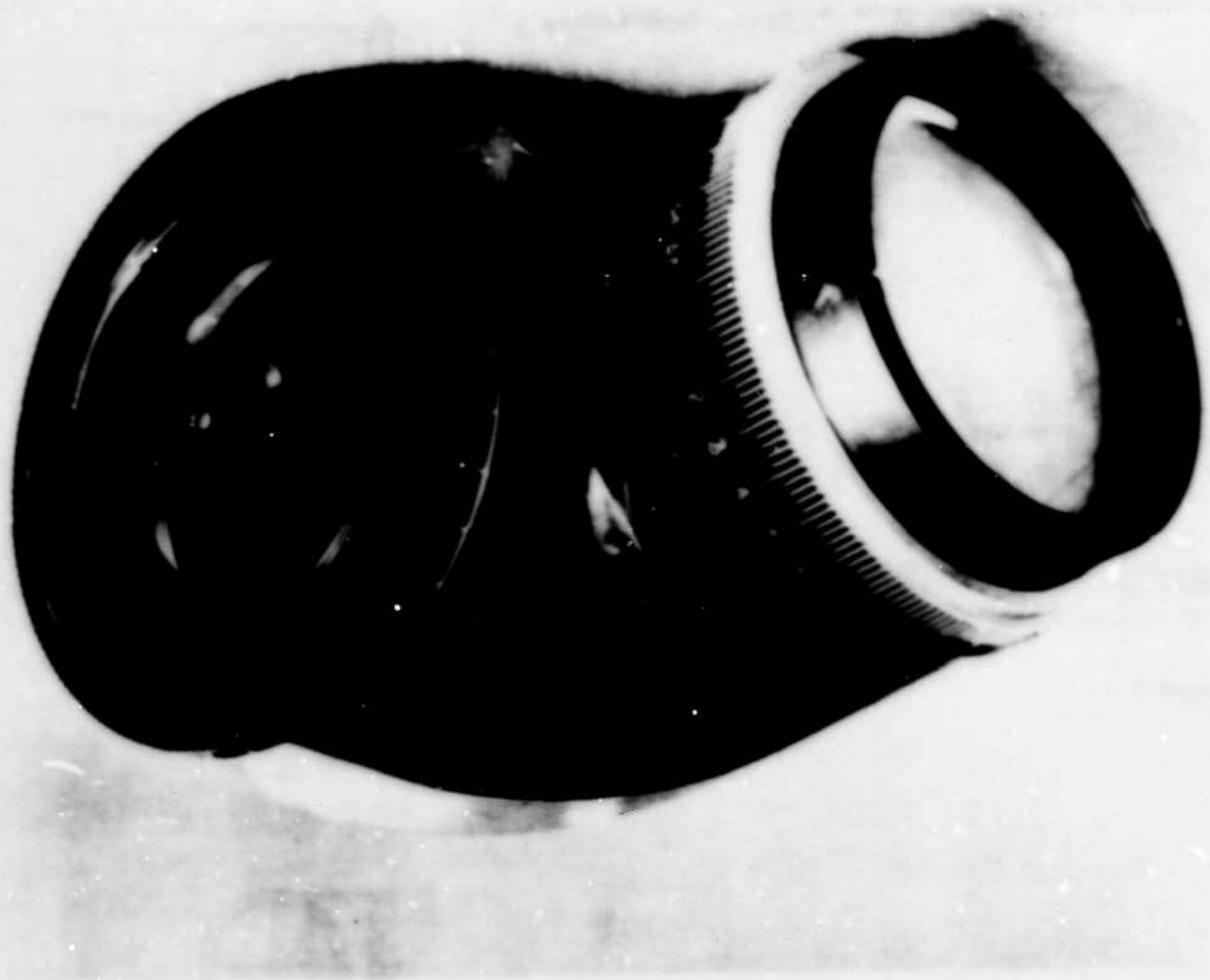


Figure 3-2. Photo of Visible Collimator Module

3.3 THERMAL DESIGN CONSIDERATIONS

The Visible Collimator, being an optical module, does not contribute to the system thermal heat dissipation problem. However, the module must be taken into account in the system thermal design. Temperatures generated by adjacent modules heating the optical elements can offset the index of refraction of the lens elements. The possible effects of temprature on the optical elemnts are described in the detailed discussion of the system thermal design considerations provided in Section III of Chapter I.

3.4 OPTICAL INTERFACE DATA

Figure 3-3 is an optical layout of the visible collimator and Table 3-1 gives the prescription for the optical design. The layout has been unfolded around the turning mirror. Although the clear aperture of the first element is 1.58 inches, the specified resolution is obtained using a 1.213 inch diameter bundle. It should be noted that the prescription and layout are based on a stop placed so far forward as to cause a slight vignetting at the ends of the LED array. This is shown by the values of the clear apertures given. The actual CA of the first surface of element 3 is 1.58 inches, vs. 1.60 inches in the table. A FLIR will usually be designed with visible optical elements in addition to a scanner and visible collimator. The position and size of the stop will be determined by the size, number and position of these additional elements, The optimum performance of the system will be obtained by trading off the stop parameters against the amount of viguetting the designer is willing to allow.

The design has been included so that it may be incorporated into the design of any system unique optics such as eyepieces or relay lenses, but it may be useful first to consider any problems or restrictions involved in using the visual collimator alone (with the LED & scanner modules) to produce a visual display.

One drawback to this configuration is that the system magnification is limited to the magnification of the infrared afocal (if any) which is likely to be less than that considered acceptable for military systems. Another

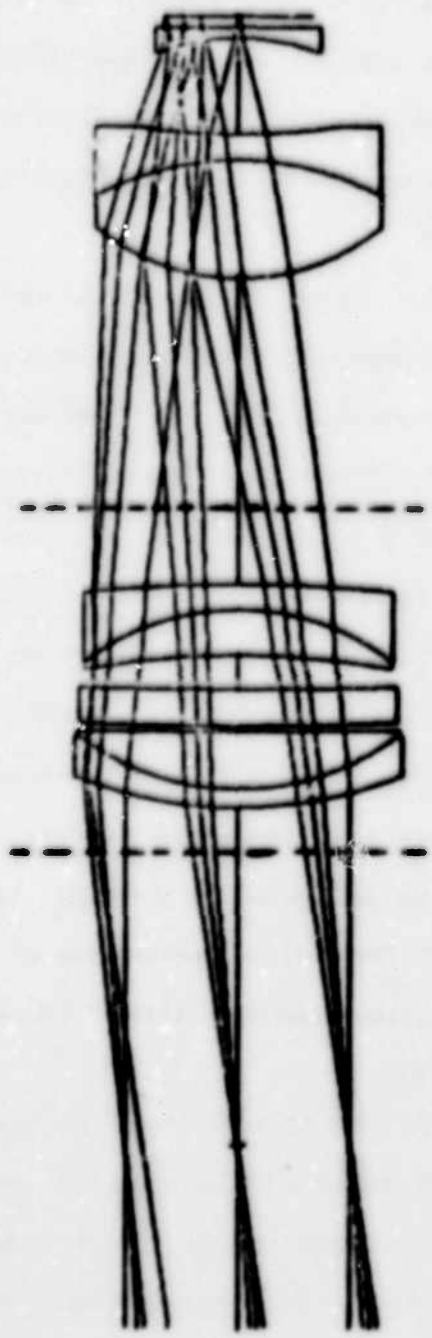


Figure 3-5. Visual Collimator Optical Layout

ELEMENT	R_1	R_2	T	CA_1	CA_2	GLASS
			APERTURE STOP	1.2150		
			1.8400			
1	2.3180	1.9050	.1000	1.6557	1.6237	F2
2	1.9050	136.7500	.3190	1.6237	1.6143	SK2
			.0251			
3	17.1550	26.5320	.2000	1.6048	1.5702	SK2
			.1810			
4	-4.4190	-1.3307	.2500	1.5439	1.5427	SK2
5	-1.3307	-7.6360	.1380	1.5427	1.5353	F2
			1.6674			
6	1.1903	-1.5870	.6430	1.4253	1.2696	SK2
7	-1.5870	3.9586	.1400	1.2696	1.0948	F2
			.5195			
8	-1.2000	INF	.0600	.8092	.7842	F2
			.0638			
	DEFOCUSING	=	-.0038			
IMAGE		INF		.7874		

NOTE - POSITIVE RADIUS INDICATES THE CENTER OF CURVATURE IS TO THE RIGHT
NEGATIVE RADIUS INDICATES THE CENTER OF CURVATURE IS TO THE LEFT

- DIMENSIONS ARE GIVEN IN INCHES

EFL	=	2.6690
BFL	=	.0638
FFL	=	-2.0754
F/NO	=	2.2003
OAL	=	6.0963
SEMI-FIELD ANGLE	=	8.3911
ENTR PUPIL DIAMETER	=	1.2130
ENTR PUPIL DISTANCE	=	0.0000
EXIT PUPIL DIAMETER	=	1.5599
EXIT PUPIL DISTANCE	=	-3.3685

Table 3-1. Visual Collimator Prescription

drawback is that the essential resolution element size is about twice what the eye can resolve under lab test conditions. Under the stress of battlefield conditions, the display should be presented larger to make it easier for the operator to gather the information in it.

The diopter correction is hard to provide under these conditions. It would have to be done by moving the LED array with respect to the visible collimator causing the scan mirror to scan non-parallel light and causing mechanical interference for negative diopter settings.

Figure 3-4 indicates another problem with direct viewing. The scan module is shown with a 1.58 inch bundle coming into the scan module. The position in which the eye must be placed in order to have a ten-millimeter eye ring is well within nose-bumping distance of the scan module, and this is the most open configuration possible.

In systems which use an eyepiece, vidicon or I^2 tube, auxiliary system unique optics must be added. In some cases, the phase shift lens can be incorporated into this design, thus serving two purposes - correcting the phase shift caused by the channel electronics and focusing the output of the visual collimating module where it can be collected by an image tube or examined by an eyepiece. The peak-to-peak motion of this phase shift lens is about .002 inch maximum.

One has some freedom in choosing the phase shift lens parameters in order to fulfill both phase shaft and visible collimator interfacing functions. The power in this lens can probably vary by ±10 percent without doing serious damage to the system MTF - the power for this lens is chosen as a median value for a wide dispersion of individual channel caused phase shift displacements. The lens power is a compromise for all channels and all frequencies. One is also allowed to place the lens at different positions in the interlace gimbal,

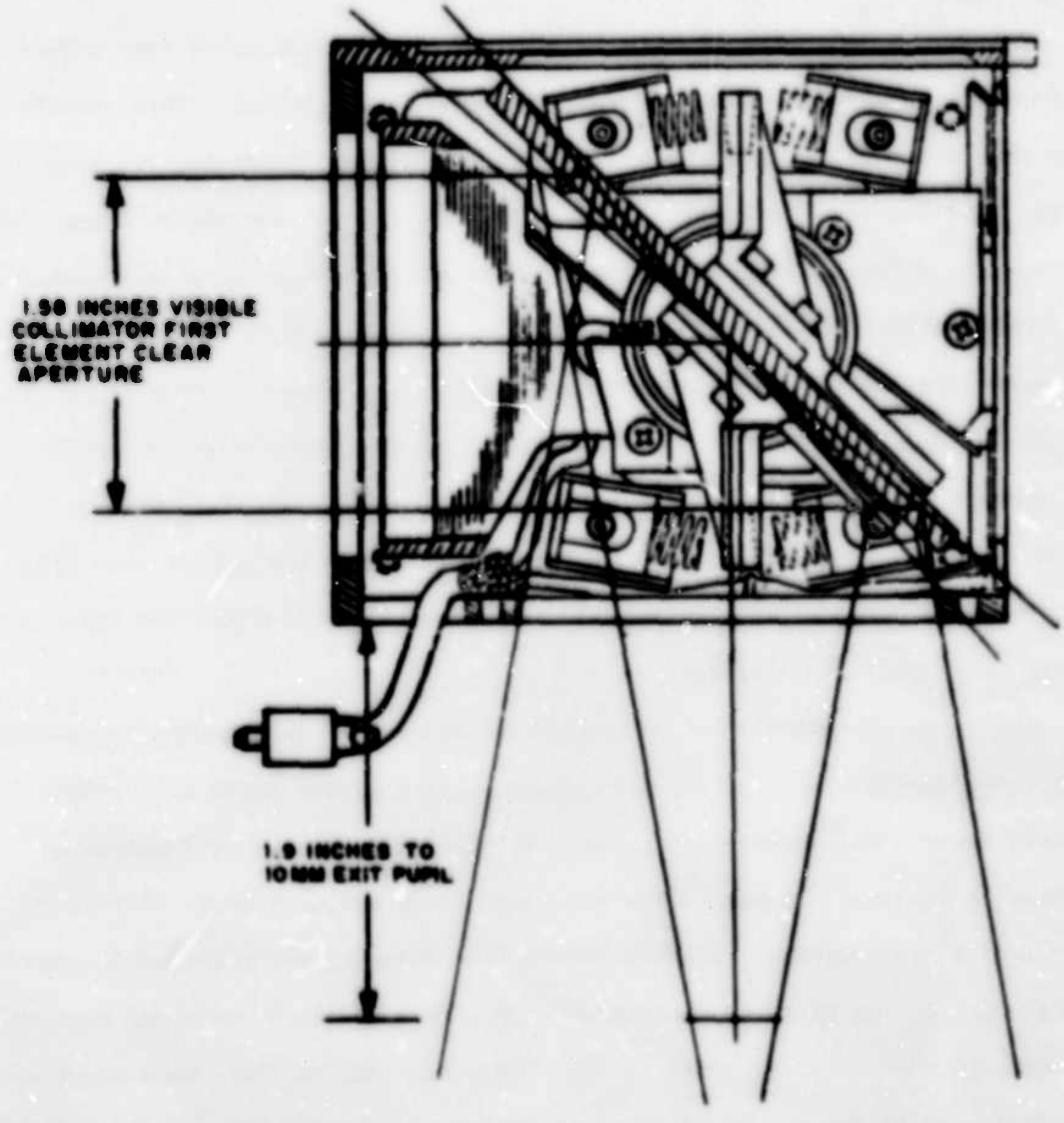


Figure 3-4. Visible Collimator & Scanner Used in Direct View

yielding at least a ±2 percent change in affect from the middle position of the radius arm.

Finally, one is free to choose the power of the phase shift lens either positive or negative in order to produce a given displacement. This results from the fact that the gimbal position does not mandate which way the scan mirror must travel. The mirror can scan the top line of the raster either left-to-right or right-to-left, depending on which way a pair of wires are hooked up.

Phase shift lens powers range from about five inches for a maximum-azimuthal scan at 60 complete frames per second, to perhaps as much as 75 inches for a five degree horizontal field scanned at 20 complete frames per second, for example. In the latter case the phase shift lens may just as well be dispensed with. Note that a good decentering tolerance for a five-inch focal length on the order of .001, which shows that we need not expect the phase shift motion to degrade the imaging.

The focus characteristics of the visual collimator do not change appreciably with temperature. This is important, because in a system built with common modules there are theoretically as many as four different optical causes of defocusing - afocal thermal shifts and range focus misadjustment, IR imager "athermalization" defocus, visible optics link defocus, and eyepiece diopter misadjustment. An operator confronted with a fuzzy picture would not know which one to adjust in order to clear it up. The visual optics link, once adjusted, should remain in focus. Other remedies include athermalization of the infrared afocal, providing a fixed-diopter display, and using a temperature servo-controlled athermalization focus on the IR imager.

In this connection, it is recommended that initial set-up focus for the visual optics be provided for in the system unique optics and not by such measures as shimming the LED module - visible collimator interface.

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the alignment and maintenance requirements to be considered in the use and application of the Visual Collimator Module. Presented herein are the test equipment requirements, alignment techniques, and maintenance information

4.2 ALIGNMENT

The assembly of the turning mirror to the visual collimator assembly is the means of controlling both the angle of deviation and the centering of the output relative to the input. In order to accomplish this during assembly it must be possible for the input to be controlled and the output to be observed. The effect of adjustment of the turning mirror can then be immediately noted and fed back so as to assure proper positioning before the silicone rubber sets. The same instrumentation without need for the mirror clamping fixture, should be used to test a completed module for proper deviation and centering.

An advantage of the following method of alignment is that without shifting his head, the operator may see all the data required for the proper alignment of the visual collimator. The turning mirror translation and tilt degrees of freedom are likely to be somewhat interactive in their effects, so that repeated adjustments will be necessary. A combined readout of centering and deviation such as this will minimize adjustment steps and reduce operator fatigue.

4.2.1 PRIMARY DESCRIPTION OF FIXTURES AND METHOD

There are three main assemblies in the visible collimator test station. Figure 4-1 shows a schematic representation of these assemblies consisting of a source assembly, a visible collimator and turning mirror clamping fixture, and a readout assembly.

4.2.1.1 Clamping Fixture

Since silicone rubber will take 24 hours to set securely, the mirror adjustment fixture must also serve as a clamp for this time period. In a production environment several modules per day will have to be assembled, so that the clamping fixture should be separable from the rest of the instrumentation. Then multiple clamping fixtures may be cycled through the set-up. High precision parts are held to a minimum on the clamping fixture. The precision parts are in the source assembly and the microscope assembly.

4.2.1.2 Source Assembly

The source assembly consists of an LED or some other source of 0.66 micrometer radiation, condensing optics, a ring reticle placed approximately six inches from the flange of the collimator, a crosshair reticle placed at the focal plane of the visible collimator (slightly displaced from the specified value of back focus due to the absence of the LED field flattener) and a collar which when placed on the pilot at the rear flange of the collimator positions the reticles on a line which is normal to the flat of the flange and centered with respect to the pilot. The reticles are adjustable for focus if necessary.

4.2.1.3 Readout Assembly

The readout assembly consists of two subassemblies, the microscope-base plate subassembly and the graticule unit. The graticule unit is attached to the front pilot of the visual collimator and the microscope allows the operator

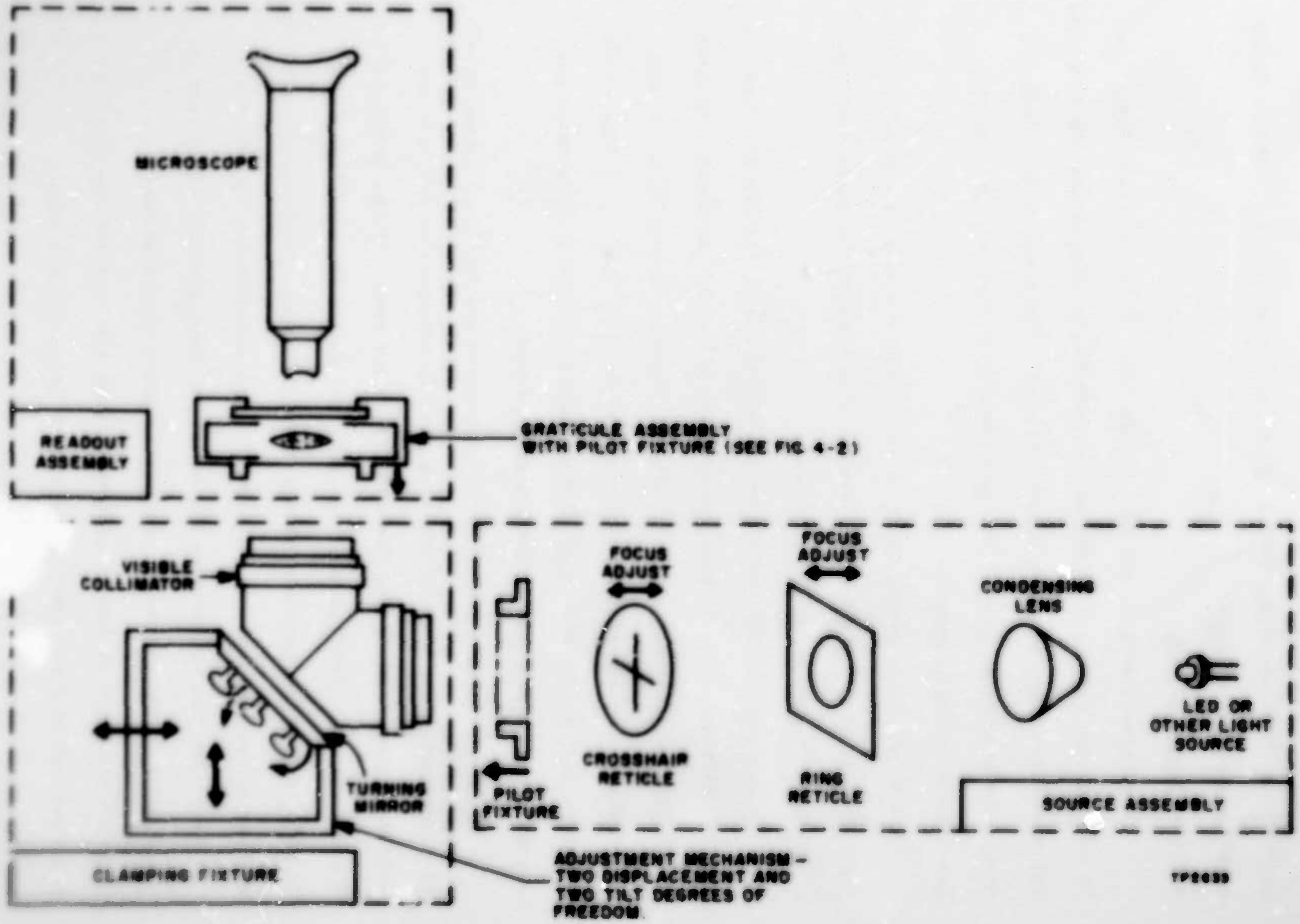
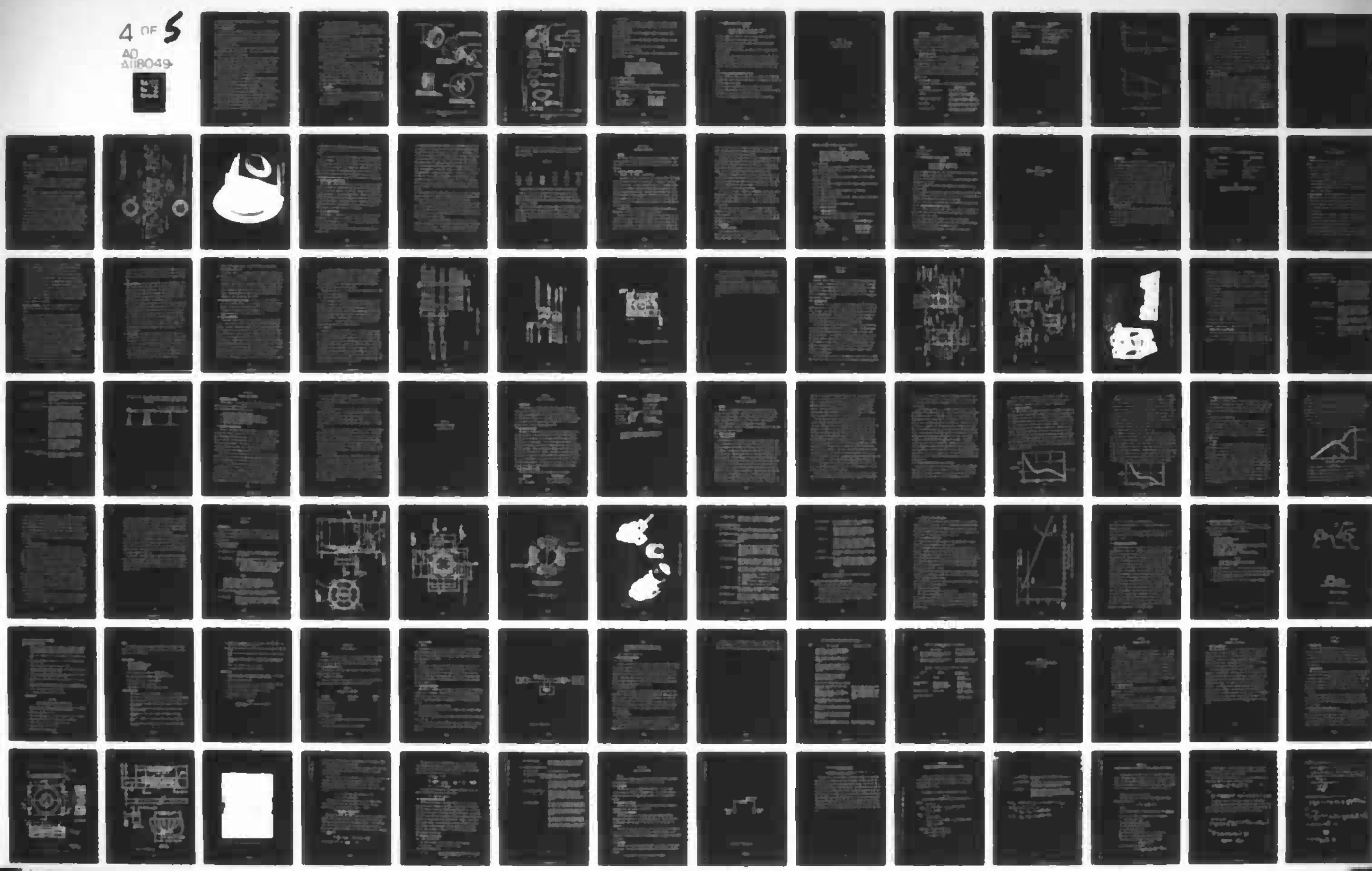


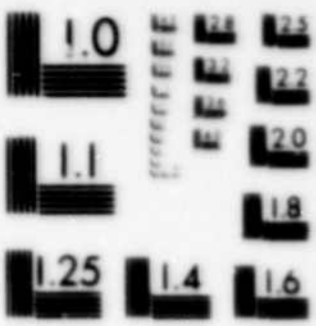
Figure 4-1. Visible Collimator Alignment and Test Fixture

AD-A118 049 MAGNAVOX GOVERNMENT AND INDUSTRIAL ELECTRONICS CO MA--ETC F/G 9/5
PRELIMINARY COMMON MODULE DESIGN HANDBOOK.(U)
APR 76 DAAG53-75-C-0178
UNCLASSIFIED GSDR-900 NL

4 OF 5
AD
A118049



18049



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

to view the position of the images formed on the graticule. The microscope need not have a crosshair.

4.2.1.4 <u>Graticule Unit</u>

The graticule unit is shown in Figure 4-2. It has two functions. One is to place the graticule in the proper position to demonstrate the centering and normality of the emerging bundles of rays. The other is to adjust the focus of the emergent bundle from each reticle so that they are parfocal and focused on the graticule.

The image of the ring reticle is at a short finite distance outside the front element of the visible collimator. This requires no additional power to bring it to a focus on the graticule.

The crosshair object reticle is collimated by the visible collimator so that an additional lens is required to bring this image to focus. In order to provide two different paths for the two images, a beamsplitter is used to deflect the collimated bundle out of the axial direction. A lens in the graticule unit brings the image of the crosshair object to a focus on the graticule via another bounce off the beamsplitter.

The image of the crosshair will demonstrate the degree of centering of the output ray. The image of the ring reticle demonstrates how well the visible collimator meets the 90-degree deviation spec. If the graticule is direct reading in thousandths of an inch, the degree of centering can be directly read by the operator through the microscope. Errors in deviation will be shown by reading the ring position in x & y coordinates, finding the resultant, and then dividing by the effective image distance (which can be calculated once for the set-up and used for every module tested).

When the setup is used for alignment, both the ring and the crosshair images are set at zero (the intersection of the graticule axes).

4.2.2 POSSIBLE CONFIGURATION FOR TEST STATION

One possible embodiment of these assemblies is shown in Figure 4-3. This set-up depends upon reducing the weight and size of the clamping fixture so that it can be attached to the visible collimator, rather than the collimator being attached to the clamping fixture.

The advantage gained is the elimination of precision machinery needed to position the visible collimator and a massive clamping fixture to the source assembly in order that the rear pilot is seated without strain. If the clamping fixture rides along with the visual collimator, only lower precision uncalibrated setscrews are needed, those for the turning mirror position adjustment. This also minimizes the amount of material and work to be repeated for multiple clamping fixtures.

A lanyard and cushion are used to control the location of the separate graticule unit when it is not attached to a visible collimator.

Since the visual collimating module and the IR imaging module are similar in field of view, size, and configuration, it is possible to construct a common source assembly. This is indicated in Fig. 4-3. Using zinc sulfide for reticles and condenser and an incandescent source would allow conversion by simply replacing the filter and an adaptive flange for mounting the module.

4.3 MAINTENANCE

4.3.1 GENERAL MAINTENANCE

The maintenance function required for the Visible Collimator module are inspection for mechanical damage and cleaning both metal and lens surfaces when needed. When both metal and lens surfaces require cleaning, the metal surfaces should be cleaned first.

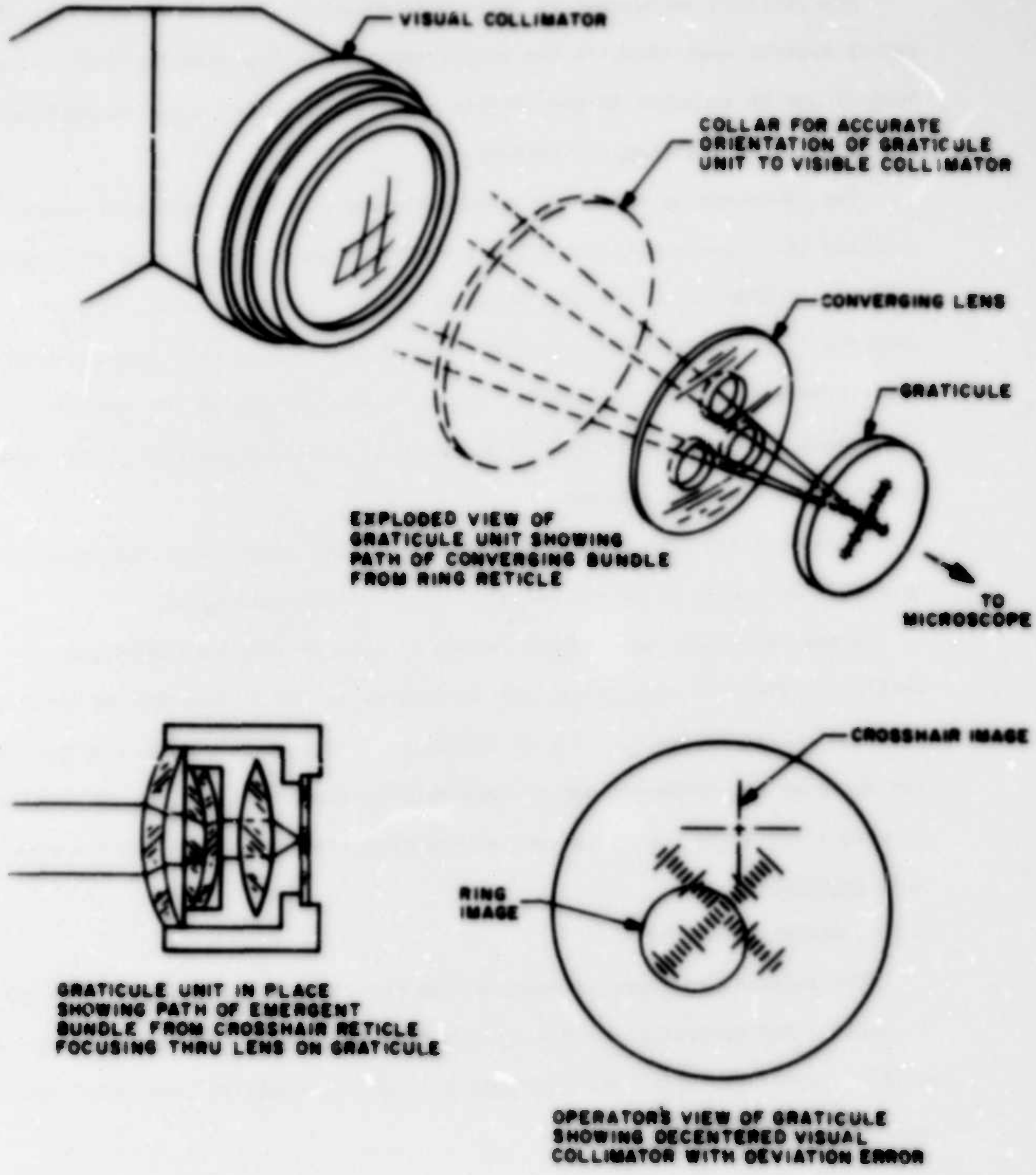


Figure 4-2. Graticule Unit of Visible Collimator Alignment Fixture

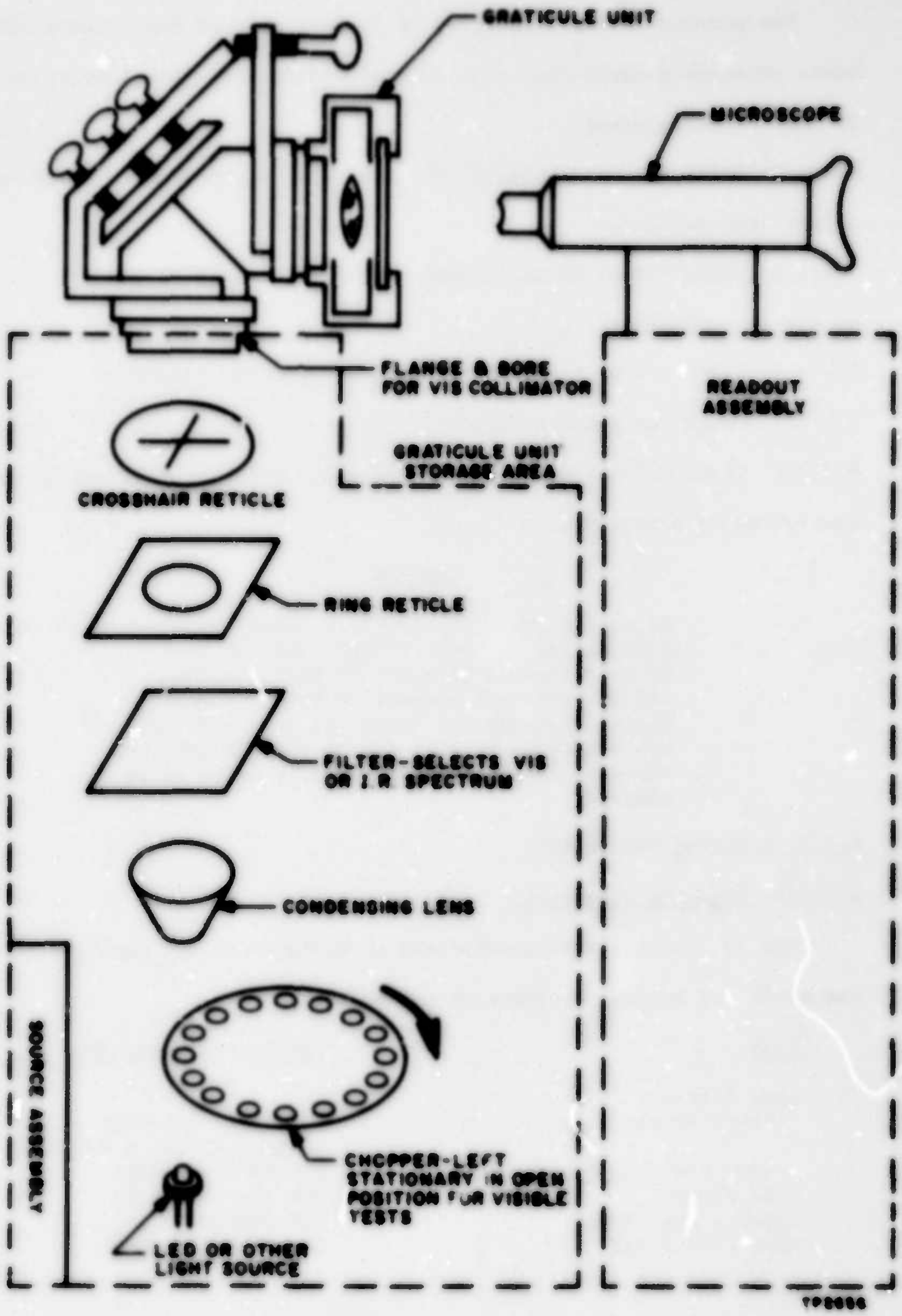


Figure 4-3. Possible Configuration for Visible Collimator Test Station

4.3.2 INSPECTION

The purpose of the inspection is to determine if the Visible Collimator meets acceptable mechanical requirements before use. The inspection consist. of the following steps.

4.3.2.1 Check the metal housing for excessive dents or warp which might effect lens position.

4.3.2.2 Check lenses of the system for chips, cracks or excessive scratches on the lens coatings.

4.3.2.3 Check mirror for signs of cracks, chip or scratches.

4.3.2.4 Check for missing screws.

4.3.2.5 Check all surfaces for cleanliness. Clean if required as described in the following paragraphs.

CAUTION

> Do not be too eager to clean lenses if they appear to have a little dust on them. It will take quite a bit of dust to block off as much as 1 percent of the throughput. Before transmission tests and when modules are assembled in to a system for delivery are the only times the lenses really ought to be cleaned.

4.3.3 CLEANING PROCEDURES

4.3.3.1 Cleaning Materials

The following cleaning materials or equivalents are required for cleaning the metal and optical surfaces of the module.

Item	FSN or FED Spec. No.
Lens Cleaners	
Ethyl Alcohol	FED Spec. O-E-760b Grade 1, Class A or B
Lens Cleaning Fluid	FSN 6810-201-0906
Lens Tissue	FSN 6640-507-6745
Camel's Hair Brush	FSN 7920-205-0565
Lint-Free Cloth	FSN 8365-170-5060

4.3.3.2 Cleaning Lens or Mirror Surfaces

CAUTION

> Use lens tissue when cleaning lens or mirror surfaces. DO NOT use a cloth which might scratch the lens or mirror surface

4.3.3.2.1 Remove all loose dirt, dust and foreign matter from the lens or mirror surface with a clean camel's hair brush.

4.3.3.2.2 Fold lens tissue to form a swab. Avoid touching the swab cleaning surface with the fingers.

4.3.3.2.3 Squeeze a few drops of lens cleaning fluid or alcohol onto the optical surface.

4.3.3.2.4 Gently wipe the optical element surface carefully with the lens tissue swab preferably in a circular motion and with very light pressure starting from the center of the surface and working towards the outer edge.

4.3.3.2.5 Allow to dry or wipe away excess cleaning fluid with a second swab.

4.3.3.3 Cleaning Metal or Exterior Surfaces

4.3.3.3.1 Remove all loose dirt, dust and foreign matter from the exposed surfaces with a gentle blast of clean moisture free compressed air (25 lbs max) or with a camel's hair brush.

4.3.3.3.2 Wipe all exposed surfaces with a clean, lint-free cloth.

4.3.3.3.3 Remove stubborn or ground in dirt with a cloth dampened with clean fresh water or a mild solution of detergent and water.

4.3.3.3.4 Dry the surfaces thoroughly with a clean lint-free cloth.

CHAPTER 10

IMAGER, OPTICAL, INFRARED

USAECOM SM-C-773419

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Infrared Optical Imager common module, hereinafter called the IR Imager, focuses the IR radiation energy from the scan mirror of the Mechanical Scanner module onto the IR detector array of the Detector/Dewar module. A position gear ring permits the imaging lens to be repositioned or focused by an external drive assembly to ensure maximum image definition.

1.2 INTENDED USE OF ITEM

The IR Imager has been designed to be interfaced with other major common and special modules to form an integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The IR Imager is optically interfaced between the mechanical scanner and the detector/dewar modules. The function of the IR Imager is to receive the parallel beam IR radiation bundle from the scan mirror, turn the bundle 90°, and direct the energy onto the elements of the detector array.

1.3 TECHNICAL SPECIFICATIONS

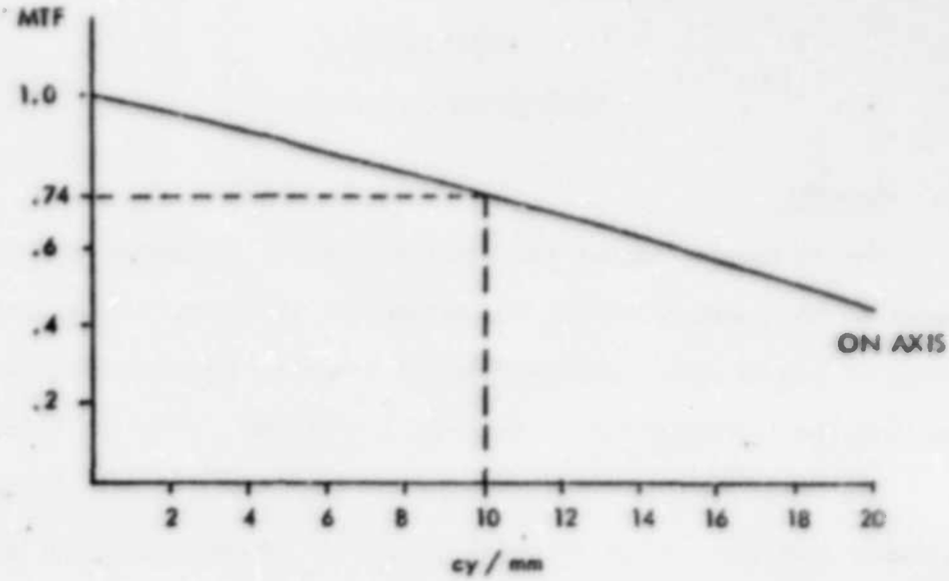
The technical specifications of the IR Imager module are as follows:

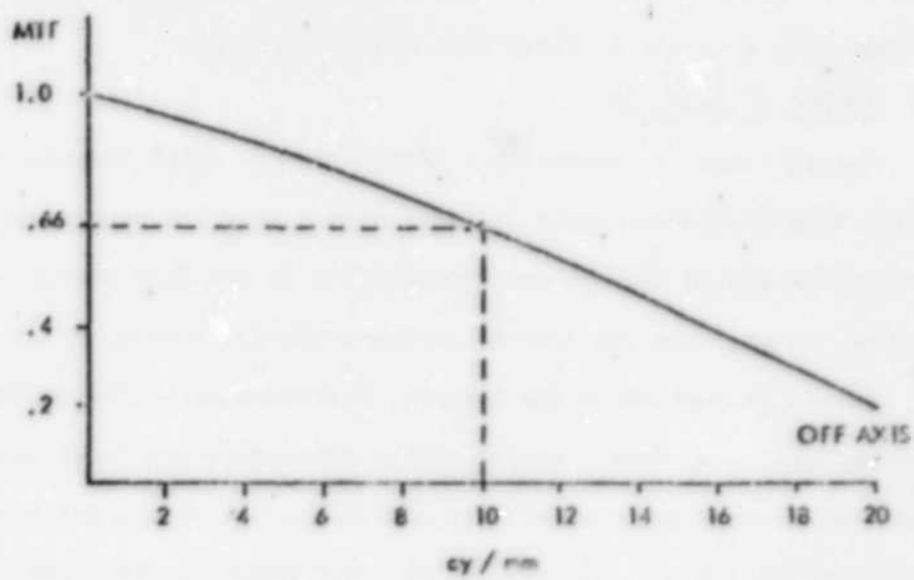
Parameter	Specification
Effective Focal Length (EFL)	67.8 ±0.7 millimeters
F/Number	Faster than F/1.8 with external stop 60 mm in front of lenses
Flange Focal Distance (FD)	17.86 ±0.25 millimeters (measured thru detector window to focal plane)
Focus Range	Adjustable 20 meters to infinity (∞) (with variation in FD of ±0.5 mm)
Field of View (FOV)	Sufficient to fill circular format with diameter of 20 millimeters

Parameter	Specification
Modulation Transfer Function (MTF)	See Figure 1-1
Linear Distortion	between 4% pincushion and 4% barrel
Relative Illumination	$\geq$60% at edge of 20 mm Field
Optical Transmittance	$>$85% in spectral region of 7.6 to 11.75 micrometers
Deviation	90° ±0.5° (degrees)

NOTE

For interface information such as mechanical configuration, outline dimensions and mounting information, refer to Section III.





B

Figure 1-1 IR Imager MTF On-Axis and 5mm Off-Axis

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The IR Imager focuses the parallel beam IR radiation received from the parallel beam scan mirror of the Mechanical IR Scanner module onto the detector array of the Detector/Dewar module. A front surfaced turning mirror is used to turn the radiation bundle at right angles (90°) onto the detector array.

The input parallel radiation end of the module mounts to the mechanical structure of the scanner by means of a pilot diameter and four attaching screws mounted in slots. This allows the designer to rotate the IR Imager about the pilot to any position within a 360 degree rotation. The group of optical elements at the input (scanner) end is axially adjustable for variable focusing through a drive. Mounting pads on either side (with dowel pin) provides means for mounting a manual or electrical drive gear train.

2.2 THEORY OF OPERATION

The IR Imager is basically a germanium lens which focuses collimated energy from the afocal scene collecting lens onto the HgCdTe detector array. The lens is coated for optimum transmission in the 8-12 micron wavelength band in order to optimize the thermal emittant characteristics of the scene and thus the overall IR portion of the system. The characteristics of the lens which must be considered from a system design standpoint are focal length, clear aperture, distortion, transmission and uniformity of transmission, field of view, and resolution. The resolution requirement is best specified by the modulation transfer function (MTF) of the lens rather than just a minimum resolution requirement. The MTF yields the resolution capability of the lens over the useful

range of spatial frequency. When specifying MTF of the lens, an error budget of MTFs for the various components, of which the lens is but one, should be specified. The lens MTF must be considerably better than the overall FLIR MTF in order to meet resolution specification. Distortion is the measure of spatial uniformity over the lens useful field of view. Distortion is usually classified by an allowable percentage of pincushion and barrel distortion.

SECTION III

INTERFACE

3.1 CONFIGURATION

Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating this module in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is a photograph of the module.

3.2 INTERCONNECTING

The IR Imager normally interfaces with the Scanner and the Detector/Dewar. It can be operated in any attitude, but must be oriented relative to the mating modules so as to provide the required IR image orientation on the detector.

The IR Imager is attached to the Scanner by screws which pass through slotted holes in the mounting flange and into threaded holes in the Scanner. An angular scale is provided on the IR Imager mounting flange to aid in installing this module in the desired orientation on the Scanner.

The IR Imager has provision for focusing. If it is to be used with fixed focus, the focus ring gear may be rotated manually for best focus at assembly and then locked by a suitable means. If the focus feature is to be used either for system focus or thermal focus compensation or both, a special focus drive mechanism must be provided to engage with the gear teeth of the lens adjustment ring (SM-C-773427). A small mounting pad is provided on each side of the module housing for attachment of a special focus drive mechanism. Whether this drive is manual or electrical, either a torque limiting drive

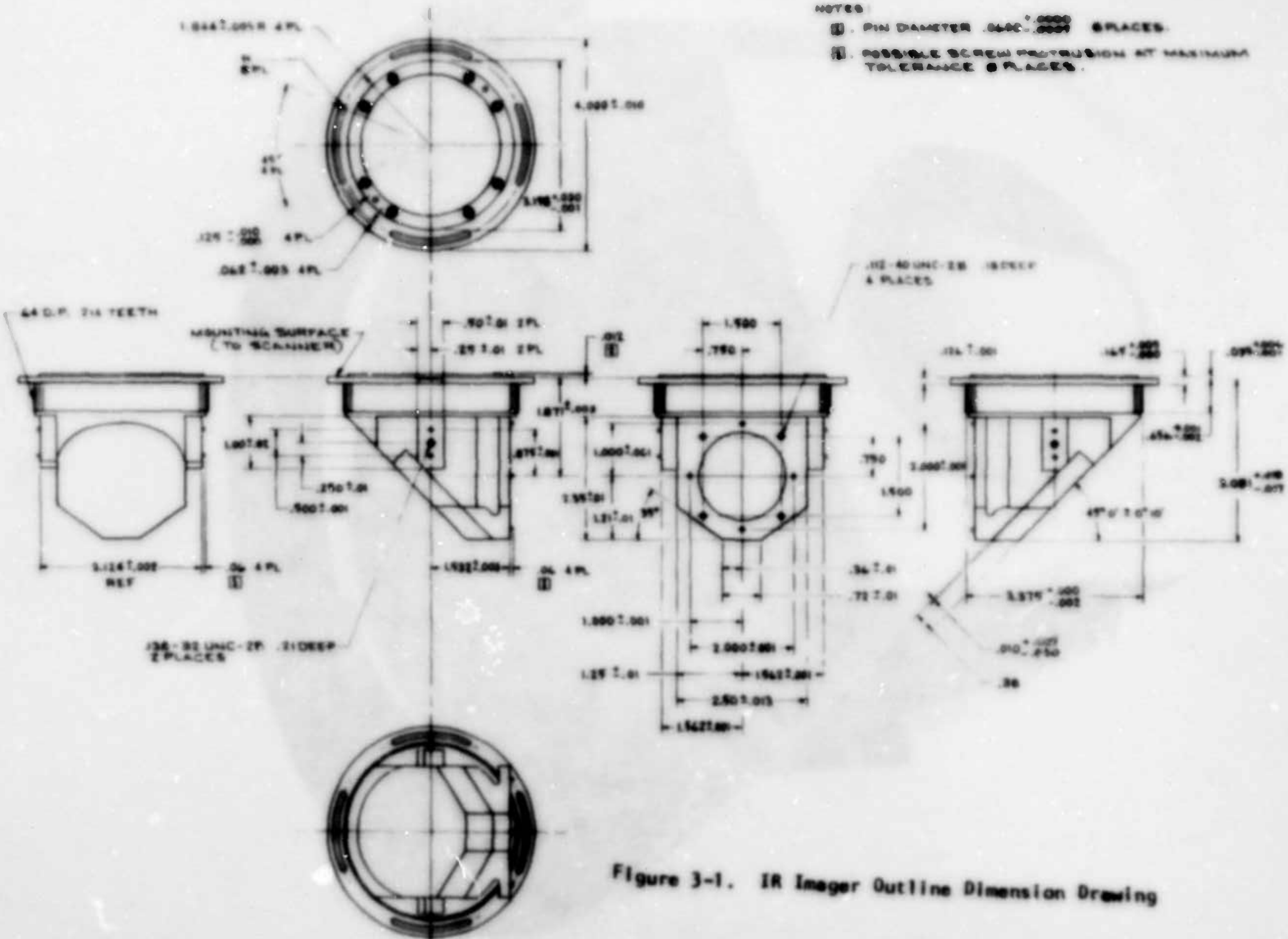


Figure 3-1. IR Imager Outline Dimension Drawing

Figure 3-2. Photo of IR Imager Module

or a separate positive stop should be used to prevent possible damage to or jamming of the moving parts of the IR Imager or of the drive mechanism itself.

There is no provision on the Detector-Dewar for direct physical connection to the IR Imager. Precise and rigid alignment of the Detector-Dewar and the IR Imager must be attained by use of a special interconnecting structure. The output mounting surface of the IR Imager, with tapped holes and locating pins, can also be used for attachment to supporting structure so that the weight of the IR Imager and any focus drive mechanism are not hung entirely on the Scanner structure which is relatively weak and subject to deflections.

3.3 THERMAL DESIGN CONSIDERATIONS

The IR Imager, being an optical module, does not contribute to the system thermal heat dissopation problem other than possibly a small amount generated by an electrical focus mechanism if one is used. However, the IR Imager must be taken into account in the system thermal design. Temperatures generated by adjacent modules heating the optical elements can affect the index of refraction of the lens elements. The possible affects of temperatures on the optical elements are described in the detailed discussion of the system thermal design considerations provided in Section III of Chpater 1.

3.4 OPTICAL INTERFACE DATA

The IR Imager is a module which focusses a parallel beam of 8-12 micron IR radiation from a scanner onto a detector. It can function alone as an objective lens of 67.8 mm focal length, F/1.8, with a half field of 8.4 degrees for a parallel beam scan system.

When designing systems involving this module, the following points should be kept in mind.

(1) The specified flange focus distance in the development spec (17.86 mm) is the physical distance in air from the rear surface of the module to the plane of best focus for the complete field of view. It corresponds to the distance to the image if there is no dewar window in the path. The physical distance from the flange to the plane of best focus when a .040 inch germanium dewar window is included in the path becomes 0.729 inch or 18.52 mm.

(2) Infrared imaging modules made by different manufacturers are at present interchangeable as to function. However, if modules of different origin are disassembled in a depot service operation or for any reason, care must be taken that the IR imaging lens assembly from one manufacturer is not reassembled to the housing from another vendor. The individual lens elements within these units are not interchangeable at present. Although the parts can be made to fit mechanically, the optical performance will not be optimum.

(3) Afocal design - In the common module system, afocal lenses collect large diameter bundles of IR radiation and compress them to small diameter bundles of parallel light for scanning, input to the IR imaging module etc.

The bundle of radiation output from the afocal is parallel only to first order optics, however, at the third order, the rays for any one point in the field are deviated from parallelism by the aberrations in the afocal lens. To the maximum extent possible, these aberrations must be balanced off by the residual aberrations in the IR imager.

Therefore, when designing afocal lenses, the IR imaging lens must be included in the computer lens design program as a fixed condition. This lens design is given in Table 3-1. If should be recognized that the mirror scanning process optically displaces and rotates the afocal groups and the IR

images group relative to each other which results in reduced symmetry and higher cost of design. However, the costs must be accepted for the resulting better optimization.

Table 3-1

R_1	R_2	T	CA_1	CA_2	Material
3.0496	3.7394	.2000	2.50	2.40	Ge
		.3110			
-14.5634	-22.0582	.1500	2.30	2.30	ZnSe
		2.3755			
1.3790	1.5722	.1350	1.70	1.60	Ge

(A germanium plate of thickness 0.040 is included in the back focus.)

ZnSe (Zinc Selenide) is available from several sources with slightly different indices of refraction. The values used in the design of the IR imager are based upon those published by Raytheon for their product, Raytran ZnSe. ($N_{9.00}$ = 2.4122)

Substitution of the product from Eastman Kodak ("Irtran 4", $N_{9.00}$ = 2.4.1.3) for example, will result in an expectation of increase of back focus by 0.0001 inch. Except for slight scattering off the grain boundries in the sintered Kodak product, other optical effects are even less significant than the back focus change.

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the IR imaging module. Presented herein is a general outline of test equipment required and the methods employed.

4.2 IR IMAGER ALIGNMENT PROCEDURE

4.2.1 ALIGNMENT & TEST FIXTURE - TURNING MIRROR

The assembly of the turning mirror to the IR imager module is the means of controlling both the angle of deviation and the centering of the output relative to the input. In order to accomplish this, during assembly it must be possible to introduce a centered and angle-controlled beam and test the output for centering and deviation. Reference should be made to the visible collimating module Designer's Handbook, alignment and test section. The infrared alignment and test is similar to that for the visible collimator, except that it is made more complicated by the necessity of using a detector to sense the radiation.

An understanding of the visible collimating module test equipment and procedure will be helpful in following the IR procedures.

A source of 7.5 to 11.75 micrometer radiation is chopped and used to illuminate a series of reticles similar to those in the visible collimator test station source assembly. Since the two modules have similar fields of view and "sensor" dimensions, it is feasible to use the same source assembly with each. As with the visible collimator, the IR imaging module is fitted into an

adapter so that the entering beam goes into the module from the focal plane side. For ease of scanning with a detector a box reticle should be used in place of the ring reticle in the source assembly.

In order to check both centering and deviation, IR images must be scanned at two different axial locations or the two images must be brought to the same scanning plane by flipping an auxiliary lens in and out. A large detector may be used without precise positioning relative to the front flange of the imager, but the scanning aperture position must be precisely known.

Checking simultaneously for both deviation and centering is not possible, so that a rapid means of shifting the auxiliary lens must be provided. With the auxiliary (positive focal length) lens out of the path, the line aperture in front of the detector will scan the image of the box reticle. The crosshair reticle image is out of focus at this time.

When the auxiliary lens is inserted on a semaphore, it will come to rest against precise stops which will insure that its optic axis is precisely aligned with the pilot fixture and the scanner. It will then be possible to inspect the focussed image of the crosshair reticle, and the box reticle will be out of focus.

The scanning aperture must be placed on a carrage with calibrated micrometers for travelling it in both the x & y directions. (The optic axis is the z direction.) The pattern peak readings for both x & y directions for both positions of the auxiliary lens are centered by the operator by means of adjustment of the turning mirror.

4.3 MAINTENANCE

4.3.1 GENERAL MAINTENANCF

The maintenance functions required for the IR imager module are inspection for mechanical damage and cleaning both metal and lens and mirror surfaces when needed. When both metal and the lens and mirror surfaces require

cleaning, the metal surfaces should be cleaned first

CAUTION

> Do not be too eager to clean lenses if they appear to have a little dust on them. It will take quite a bit of dust to block off as much as 1 percent of the throughput. Before transmission tests and when modules are assembled in to a system for delivery are the only times the lenses really ought to be cleaned.

4.3.2 INSPECTION

The purpose of the inspection is to determine if the IR imager meets acceptable mechanical requirements before use. The inspection consists of the following steps.

4.3.2.1 Check the metal housing for excessive dents or warp which might affect lens position.

4.3.2.2 Check lenses of the module for chips, cracks or excessive scratches on the lens coatings.

4.3.2.3 Check mirror for signs of cracks, chips or scratches.

4.3.2.4 Check for missing screws.

4.3.2.5 Check all surfaces for cleanliness. Clean if required as described in the following paragraphs.

4.3.2.6 Verify that the gear ring moves freely.

4.3.3 CLEANING PROCEDURES

4.3.3.1 Cleaning Materials

The following cleaning materials or equivalents are required for cleaning the metal and optical surfaces of the module.

Item	FSN or FED Spec. No.
Lens Cleaners	
Ethyl Alcohol	FED Spec O-E-760b Grade I, Class A or B
Lens Cleaning Fluid	FSN 6810-201-0906
Lens Tissue	FSN 6640-507-6745

Item	FSN or FED Spec. No.
Camel's Hair Brush	FSN 7920-205-0565
Lint-Free Cloth	FSN 8365-170-5060

4.3.3.2 Cleaning Lens or Mirror Surfaces

CAUTION

Use lens tissue when cleaning lens or mirror surfaces. DO NOT use a cloth which might scratch the lens or mirror surface.

4.3.3.2.1 Remove all loose dirt, dust, and foreign matter from the lens or mirror surface with a clean camel's hair brush.

4.3.3.2.2 Fold lens tissue to form a swab. Avoid touching the swab cleaning surface with the fingers.

4.3.3.2.3 Squeeze a few drops of lens cleaning fluid or alcohol onto the optical surface.

4.3.3.2.4 Gently wipe the optical element surface carefully with the lens tissue swab preferably in a circular motion and with very light pressure starting from the center of the surface and working towards the outer edge.

4.3.3.2.5 Allow to dry or wipe away excess cleaning fluid with a second swab.

4.3.3.3 Cleaning Metal or Exterior Surfaces

4.3.3.3.1 Remove all loose dirt, dust, and foreign matter from the exposed surfaces with a gentle blast of clean moisture free compressed air (25 lbs. max.) or with a camel's hair brush.

4.3.3.3.2 Wipe all exposed surfaces with a clean, lint-free cloth.

4.3.3.3.3 Remove stubborn or ground in dirt with a cloth dampened with clean fresh water or a mild solution of detergent and water.

4.3.3.3.4 Dry the surfaces thoroughly with a clean lint-free cloth.

CHAPTER 11

SCANNER, MECHANICAL, INFRARED

SM-D-773885

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Infrared Mechanical Scanner (hereinafter called the scanner) consists of a scan mechanism assembly and housing. The scan mechanism assembly includes a flat scan mirror, interlace gimbal, and associated drive components. The scan mirror pivots about the scan axis and oscillates about the interlace axis at the end of each scan or once every other scan to create a 2:1 interlace pattern. When the scanner is mounted in an infrared (IR) system, the front side of the scan mirror directs incoming IR energy through a set of IR imaging optics onto an array of IR detectors. The back side of the mirror directs the visual output from a light emitting diode (LED) array through a set of visible collimating optics and into a visible display optics assembly. The scan drive components consist of a variable-speed board (B2-2BA050120) for scan rates from 20 to 62 Hz, externally synchronized; or a low-power board (B2-2BA050119) for operating with 30 Hz direct-view systems.

1.2 INTENDED USE OF ITEM

The scanner module has been designed to interface with other major common and special modules to form an integrated Forward Looking Infrared (FLIR) or Thermal Imaging System. The primary function of the module is to optically scan the thermal image of objective space onto a detector array and simultaneously scan the output of an LED array and collimator to the visual output optics of a system.

1.3 TECHNICAL SPECIFICATIONS

The Technical Specifications of the scanner module are as follows:

Parameter	Specification
Maximum power	7.5 watts
Modulation Transfer Function	95%
Duty Cycle	70% at 60 Hz, 75% at 30 Hz
Maximum Active Scan Angle	±5 degrees @ 62 Hz
Effective interlace angle	0.75 mrad
Scan rate	20 Hz to 62 Hz

NOTE

Mechanical specifications involved with interface requirements are included in Section III.

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The Scanner Assembly consists of a cast aluminum housing with cover which houses a gimbal interlace subassembly which is the scanner mechanism.

(1) Housing - Three (3) external surfaces of the housing provide a mounting interface with various imaging systems. Two orthogonal surfaces are recommended for the mounting interface. Three (3) openings in the housing and one (1) opening in the cover provide apertures for directing the incoming IR energy by means of a scan mirror through a set of system IR imaging optics and directing a visible output from a LED array by means of the back side of the scan mirror to a set of system visible collimating optics.

(2) Gimbal Assembly - The gimbal assembly consists of a cast aluminum support which mounts the scan mirror assembly, two (2) brushless DC Torque motors (scan driver) two (2) push/pull solenoids (interlace action), two (2) transducer assemblies (Scan and interlace position pickoffs), a transducer bridge (printed circuit board) assembly with wiring, and other associated parts.

The gimbal assembly is suspended in the housing by means of two (2) opposed flexural pivot (frictionless bearing) assemblies on an axis which is at 30 degrees with respect to the mirror scan axis. This axis produces a mechanical action for interlace with the scan axis.

(3) Interlace Drive Solenoids - The gimbal assembly interlace motion is generated by the two push/pull solenoids which are mounted in an axially opposed position to a mounting block which is affixed to the scanner hous-

ing at final assembly. Two solenoid plunger assemblies are attached to the interlace gimbal. Travel of the plungers is governed by stop pins which are attached to a plate at the rear of each solenoid. A silicone rubber cushion is provided on the plunger assemblies to lower the audio noise level when operational. Free travel of the plungers are adjusted to 21 mils by placing shims symmetrically between the plungers and the faces of the solenoids. In operation, the solenoids when alternately energized drive in the pull condition. The stop pins are adjusted to provide the 0.75 mrad interlace angle. An occasional adjustment of the stop pins may be required to compensate for cushion wear or when changing between 30 and 60 Hz operation. However, the stop pin settings should not normally be changed during operation.

(4) Scan Mirror Assembly - The scan mirror assembly consists of a mirror, two (2) return arms with counter weights and upper and lower stub shafts.

The mirror is pyroceram. Both sides of the mirror are coated and are used optically in the system. The infrared side (that side facing out of the system) is coated for high reflectance in the 7.5 to 12.5 micron range and the rear is coated for high reflectance in the 0.63 to 0.69 micron range, both for incidence angles of 45°. The return arms are made of cast aluminum and extend away from the axis of rotation of the mirror assembly in opposite directions. Their purpose is to strike spring assemblies that are fixed to the housing causing a return force which, together with torque motors, swing the mirror in the opposite direction until they strike an opposite set of springs which repeat the cycle thus causing a scan mirror oscillation at the specified angle. Counterweights are cemented to the return arms to obtain a dynamic balance of the mirror.

The upper and lower stub shafts form part of the mirror assembly and are located on an axis through the center of the mirror, parallel with the mirror surfaces. These shafts are inserted into the center of the rotor

of the torque motors and attached by screws through flanges on the stub shafts. The mirror is assembled to the stub by cementing. The center axis of the stub shafts are accurately positioned with respect to each other.

(5) Spring Assemblies - There are two sets of four spring assemblies. One set is used for 30 Hz (Low Power) mode of operation and the other set is used for the 60 Hz (High Power) mode. The sets are made up of similar parts except that the 30 Hz set has weaker springs and has a silicone rubber pad on the free end of each spring. The purpose of these pads is to reduce the audio noise level in the low power condition.

The function of the spring assemblies is to control the total scan angle of the mirror assembly. The maximum scan angle for the 30 Hz condition is 5.5 degrees and the maximum angle for the variable 60 Hz condition is 10 degrees. The spring assemblies are individually adjustable to obtain these angles by screw slot adjustment of their mounts. They are positioned on the block to act as a return at each cycle of mirror scan as the return arms of the mirror assembly drive into them. This action causes the springs to compress hence reversing the direction as explained above.

(6) Torque Motors - The scanner has two brushless DC torque motors which are mounted on the scan axis and drive the mirror assembly. Each develop a peak torque of 1.3 ounce inches with a continuous power consumption of 2.4 watts. In the 30 Hz (Low Power) mode of operation, one motor is used for drive and the other is used as a tachometer. In the variable scan mode (20 - 62 Hz) both motors are used for driving. These motors are mounted opposite each other into the gimbal on the scan axis and their rotors are suspended along with the mirror assembly by means of

double ended flexural pivots. The center portion of the pivots is considered the fixed end.

(7) Transducers - There are two magnetoresistive transducers in the assembly. The resistance of the transducer varies as a function of the position of a steel vane moving in front of it. One transducer is mounted to the solenoid mounting block hence to the scanner housing and its vane (target) is on gimbal at the interlace drive mechanical connection. The other transducer is mounted at the scan axis with its vane (target) mounted to the gimbal. These transducers are used for picking off angular position information of the interlace and scan motions.

(8) Scan Module Printed Circuit Board - A small printed circuit board is part of the scanner assembly. It is a transducer bridge used for development of the scan and interlace position signals. It is wired in with a harness to the scanner electrical components and is terminated by a connector which ties in with the system electronics.

2.2 THEORY OF OPERATION

In the 30 Hz, fixed frequency mode of operation, the scan speed of the mirror is controlled by a velocity loop. The output of the tachometer (one torquer is used as a tachometer) is compared with the velocity command and the difference which is the velocity error signal is amplified by the torque motor amplifier which transmits corrective signals to the torque motor. The torquer in turn accelerates or decelerates the mirror until the error signal is reduced to zero. When the end of travel is reached, the limit stop springs are contacted which store and then release the kinetic energy. In other words, the mirror will bounce back from the stop. At the same time the input command to the velocity loop will also change polarity generated by an analog comparator which senses the output polarity of the tachometer. The mirror will now scan in the opposite direction until the other limit stop is contacted.

In this type of arrangement, the torquer has only to supply the energy absorbed by the turn-around mechanism at the turn-around time and supply corrective torques during the actual scan. In this system, the scan frequency is solely determined by the scan velocity and by the parameters of the turn-around mechanism. Any change in scan velocity and turn-around time will have an effect on the scan frequency.

Whenever the scan changes direction, a pulse is transmitted to the video electronics for further processing.

2.2.1 VARIABLE FREQUENCY OPERATION

An analog magnetic proximity type transducer (see Figures 2-1 and 2-2)* provides mirror position information during scan which is compared with an electronically generated position command and may be synchronized to an externally supplied Synch Pulse. The difference between these signals is amplified by the torque motor amplifier which in turn sends corrective signals to both torque motors. The torque motors in turn apply corrective torques to the Scan Mirror. A pulse is transmitted to the interlace electronics whenever the scan reverses for further processing.

2.2.2 INTERLACE

The position of the interlace gimbal is controlled by a position loop with velocity feed forward. The position of the interlace gimbal is sensed by the interlace transducer and is compared with the interlace position command. The difference between the interlace transducer output and the interlace position command, which is the position loop error signal, is amplified by a preamplifier and transmitted to the actuator amplifier. The output of the actuator amplifier which operates in current feedback mode powers the actuator which in turn applies corrective forces to the interlace gimbal. The interlace gimbal will now move until the error signal is reduced to zero. The interlace gimbal is now in the commanded position.

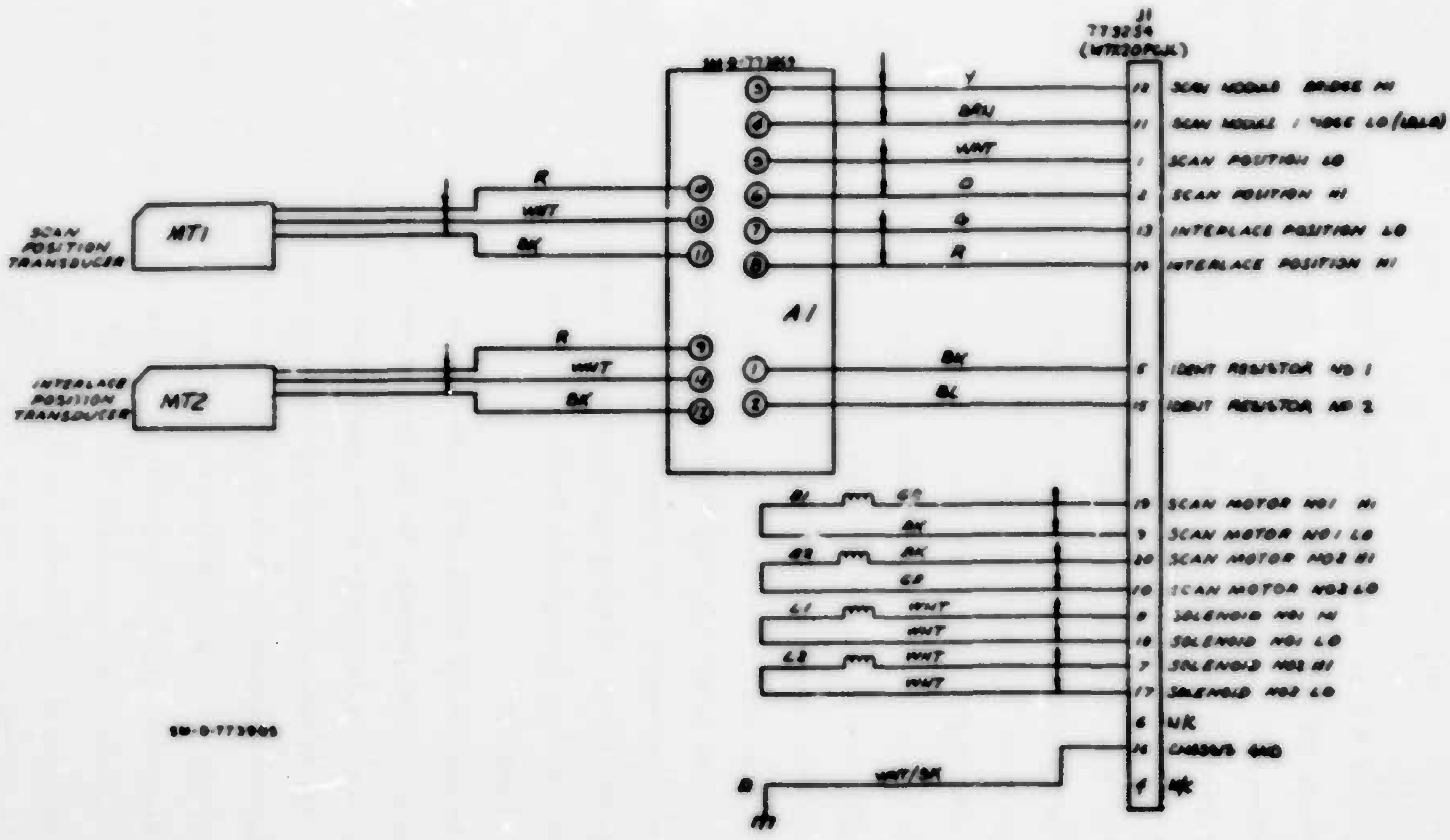


Figure 2-1. Scanner Schematic

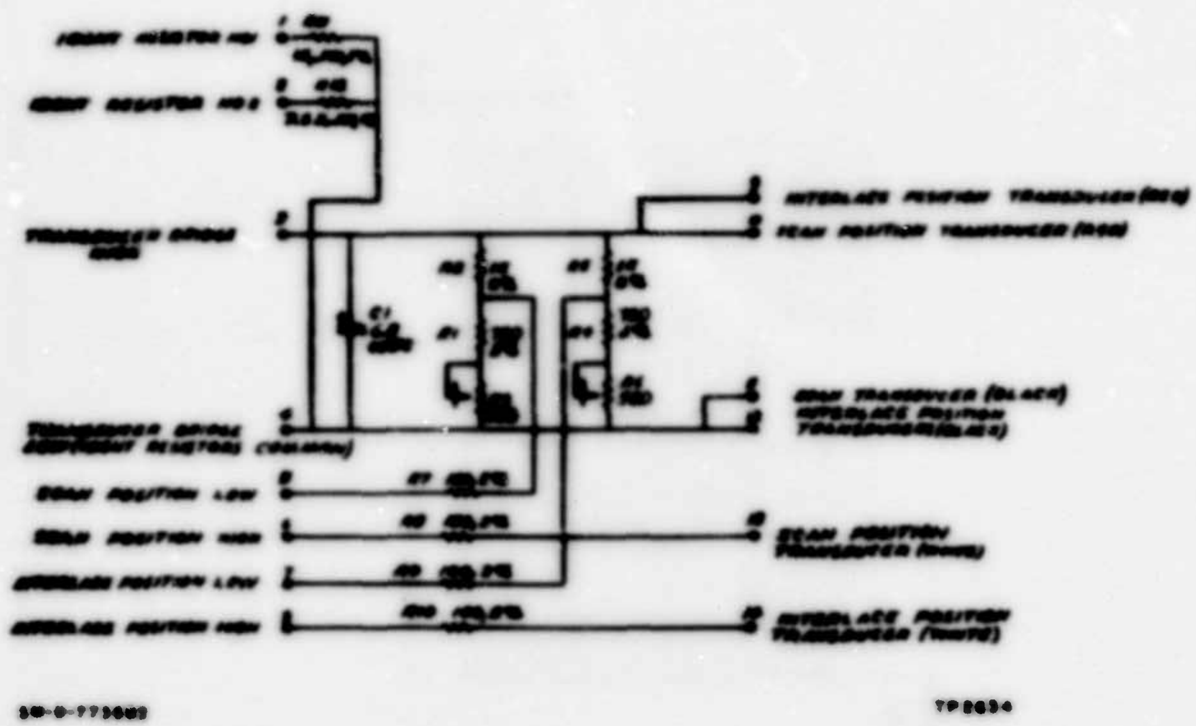


Figure 2-2. Transducer Bridge Schematic

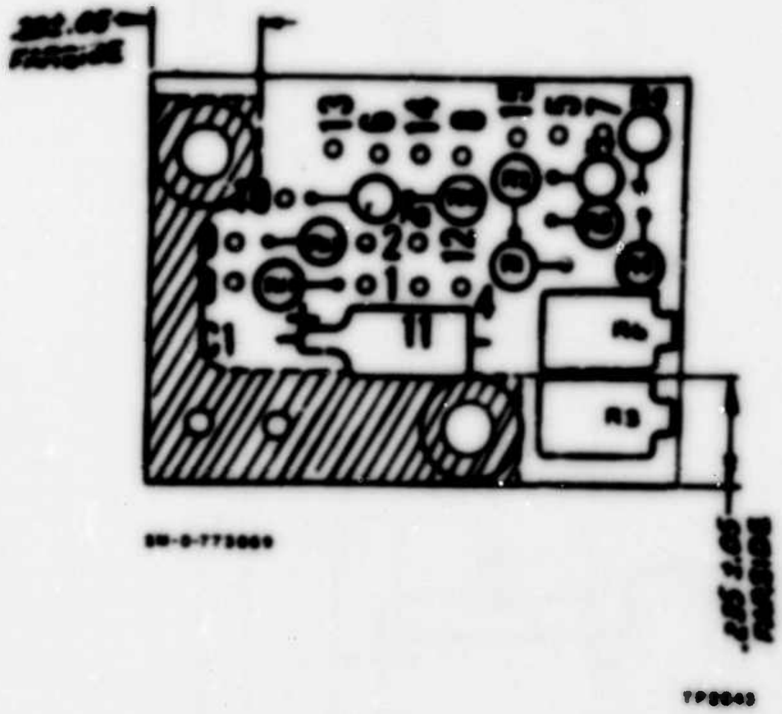


Figure 2-2. Parts Location, Transducer Bridge
(Sheet 2 of 2)

The velocity feed forward signal which is generated by the interlace electronics is fed to the preamplifier mentioned above where it is summed with the position loop error signal.

This position loop employs error rate damping for stabilization. The interlace position command is generated by a comparator which changes its output wherever the direction of the scan is reversal (once per scan mode) or when the direction of every other scan is reversed (once every other scan mode).

SECTION III

INTERFACE

3.1 CONFIGURATION

Figure 3-1 and 3-2 show the pertinent outline and mounting data for use of the designer in incorporating this module in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specifications. Figure 3-3 is a photograph of the module. Figure 3-4 is a parts location drawing of the transducer bridge assembly.

3.2 INTERCONNECTING

The Scanner normally interfaces with the IR Imager and the Visual Collimator and also with visual imaging optics and an afocal lens (if it is required in the system). The visual optics and afocal lens must be made to satisfy the unique system requirements. The Scanner can be operated in any attitude, but must be oriented relative to the mating modules so as to provide the image orientation and scan direction required for the system design.

The Scanner may be mounted to a base plate by utilizing any combination of the mounting faces indicated on the outline drawings. The scanner mounting surfaces have tapped holes as well as locating dowel pin holes. When mounting the Scanner, it is imperative that the mounting structure not strain the Scanner housing. The housing is of light-weight construction and any strain imposed on it could affect the function of the Scanner module. Consequently, consideration should be given to the use of adjustable bracket and/or shims to match exactly the mounting surfaces at assembly to avoid distortion of the housing.

Both the Collimator and the Visible Imager are in the visual optical path and, accordingly, are mounted to the housing surfaces which have openings which

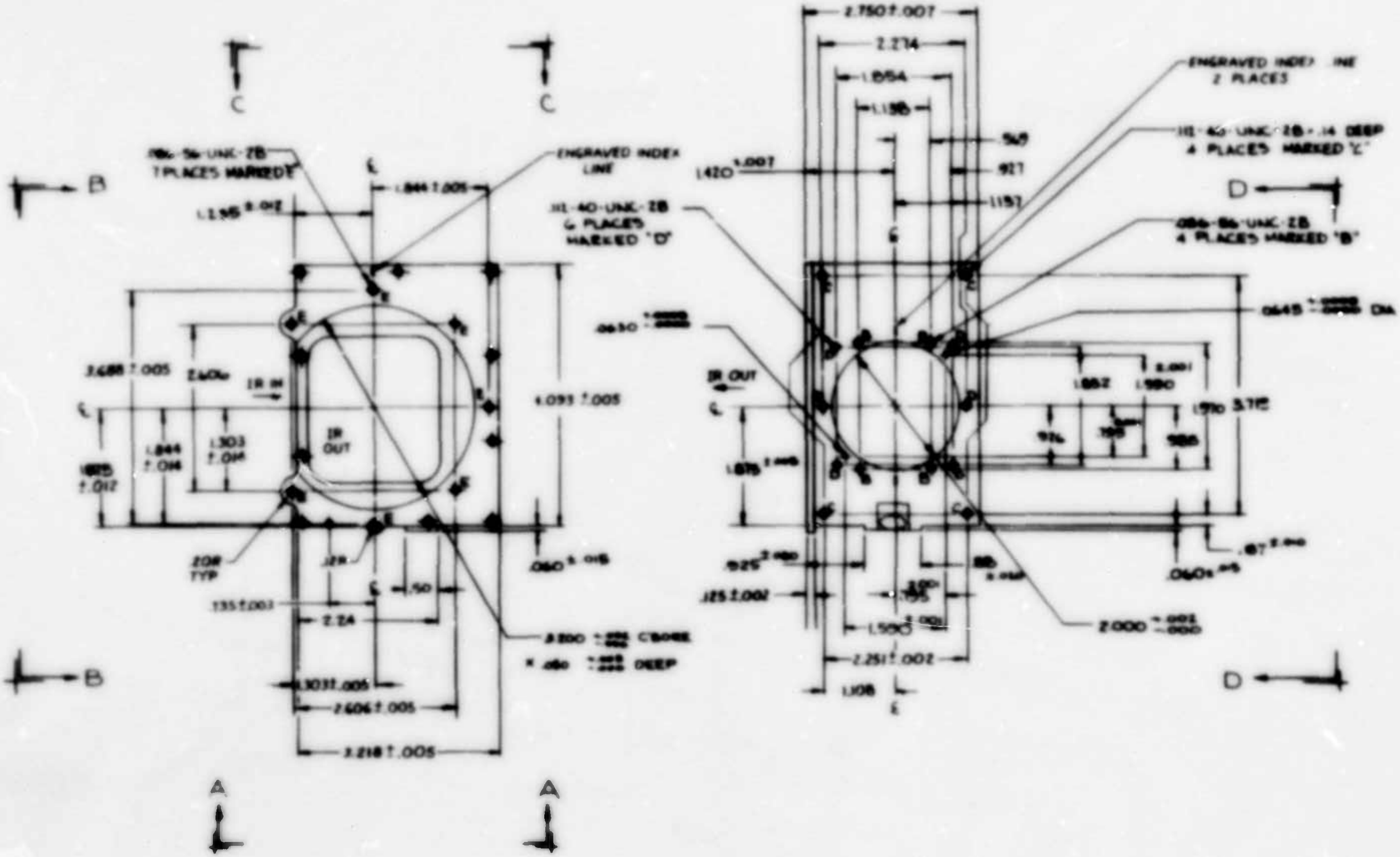


Figure 3-1. Scanner, Mechanical, Infrared, Outline Drawing

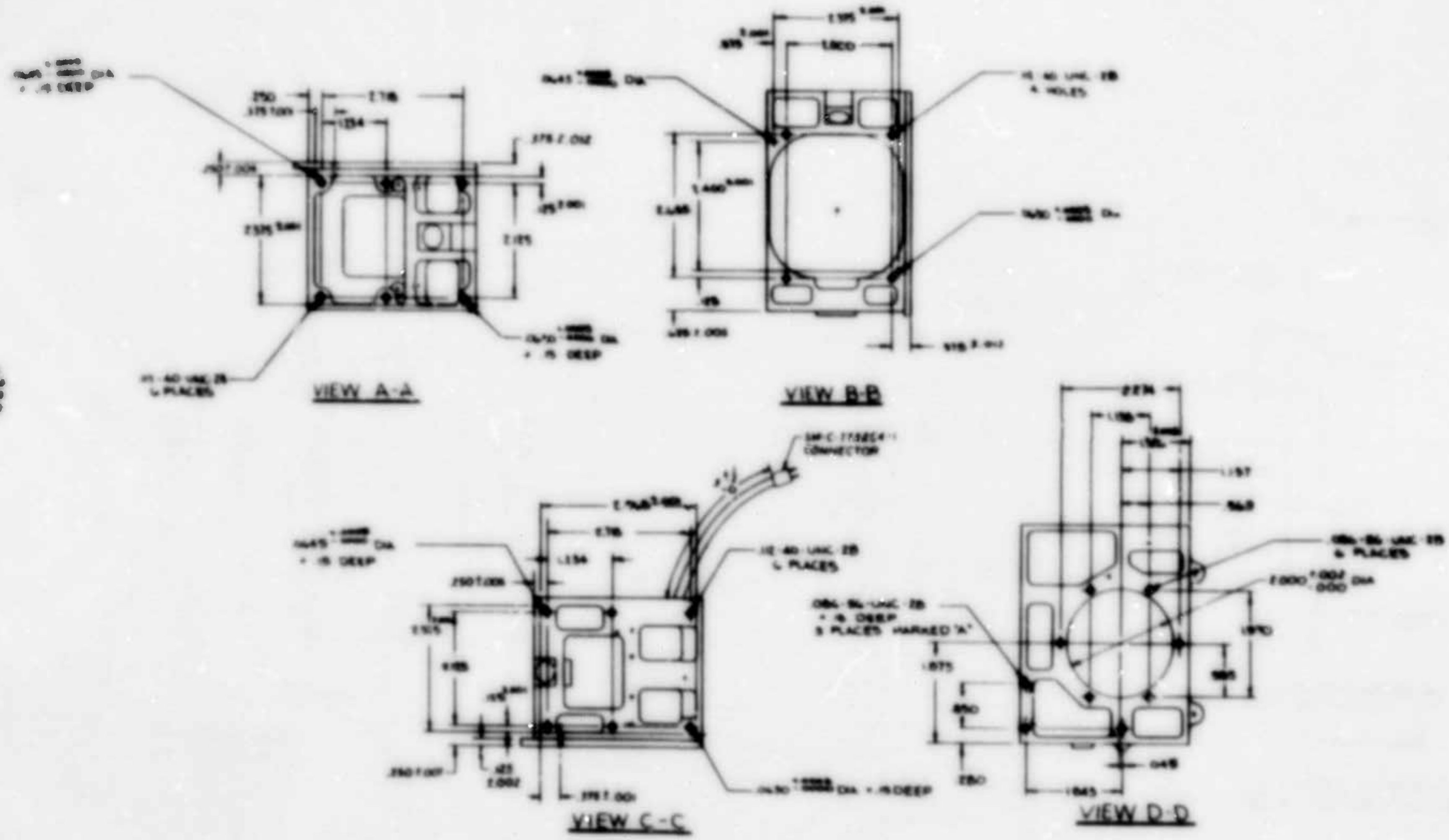


Figure 3-2. Scanner, Mechanical, Infrared Outline Drawing

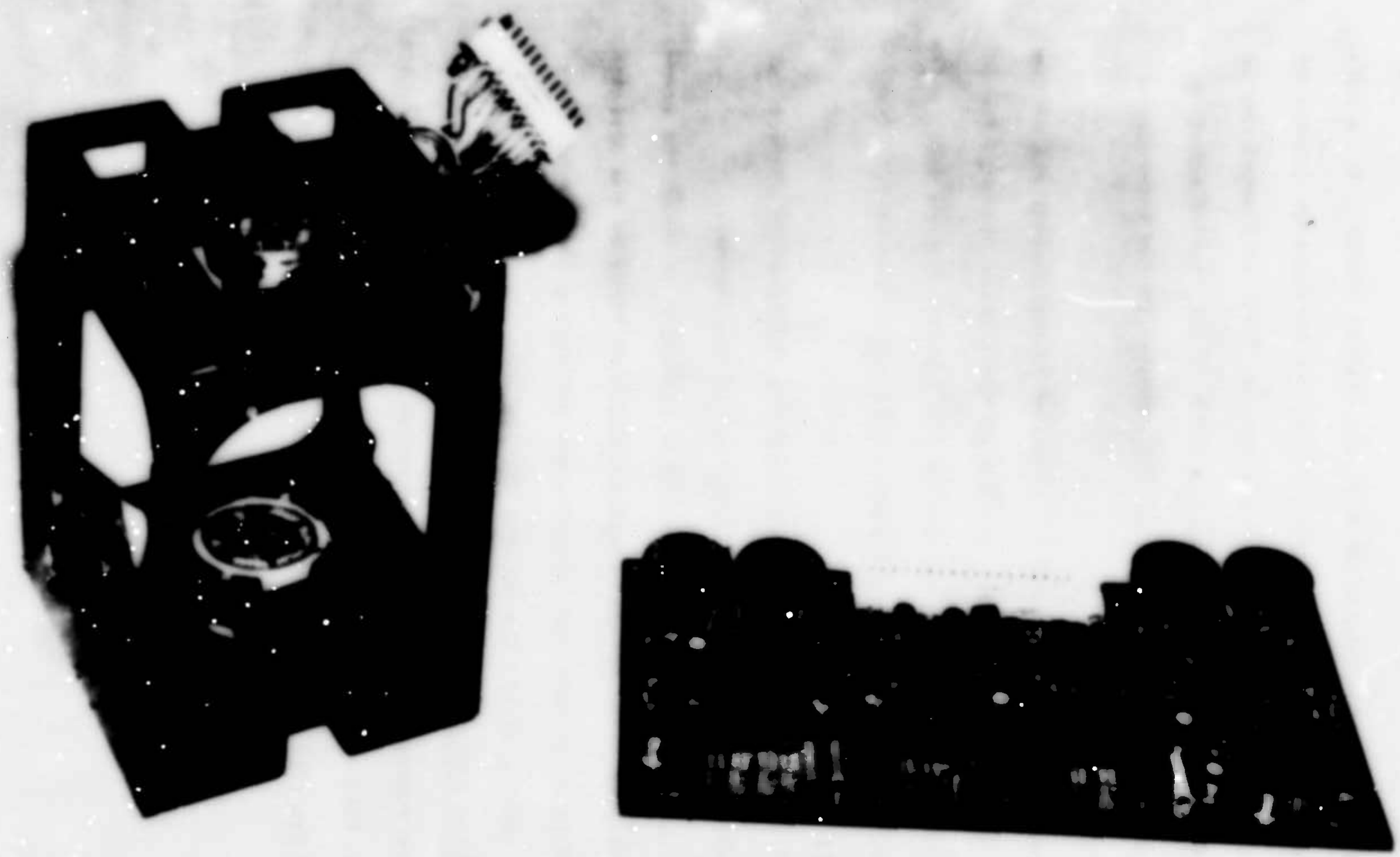


Figure 3-3. Scanner, mechanical Infrared (and Scan & Interlace Module)

face towards the visual reflecting surface of the Scanner mirror. It is permissible to mount either module to either of these two surfaces as determined by packaging design considerations. Suitable adapter rings or flanges may be required to match the Imager and Collimator modules to the housing mounting surfaces selected. See comments in Section III, Chapter 10 for interconnecting the collimator.

The IR Imager and the Afocal lens (if required by the system) are in the IR optical path with the IR reflecting surface of the Scanner mirror. The IR Imager interfaces with the mounting surface on the Scanner Housing Cover which forms one side of the Scanner Housing Assembly. See also Section III, Chapter 9 on interconnecting the IR Imager.

It is essential that the Scanner itself and the module which connect to it be mounted and supported to prevent distortion of the Scanner.

Electrical connections are made to a single connector to which the scanner harness terminates. The mating connector should be fixed by the designer in an accessible location such that plugging and unplugging the Scanner connector will not unduly strain the harness service loop.

3.3 THERMAL DESIGN CONSIDERATIONS

Although the scanner module power dissipation is relatively lower (2 watts), it must be taken into account during system design. Refer to Section II of Chapter 1 for a detailed discussion of the system thermal design considerations.

3.4 ELECTRICAL INTERFACE DATA

3.4.1 INPUT CHARACTERISTICS (60 Hz)

(a) Synchronous scan frequency:	when used with variable-speed scan board, scan frequency will be stable within 1 Hz of external sync source frequency
(b) Power:	to operate scanner and variable-speed scan board for bidirectional scanning at 30 Hz, 4 watts maximum; to operate scanner and 30 Hz low-power scan and interlace for an active mirror scan angle $\leq$ 5.50, 2.2 watts maximum; in 60 Hz bidirectional mode, 7.5 watts maximum

3.4.2 PROCESSING CHARACTERISTICS

(a) Variable scan frequency:	variable from 20 IR frames/40 fields/second to 62 IR frames/124 fields/second; nonsynchronous scan frequency drift $\leq$ 10% from ambient setting when exposed to specified staticclimates environments
(d) 30 Hz scan frequency:	adjustable to 30 ±.05 Hz; scan frequency drift $\leq$ ±3 Hz from ambient setting when expoced to specified static-climatic environments
(c) Interlace:	operates in a 2:1 interlace mode;side or rear; will interlace once per azimuth scan or once every other azimuth scan
(d) Scan direction:	operate in bidirectional mode at 2 scans per cycle

(e) Scan efficiency: minimum of 70% at 60 Hz, minimum of 75% at 30 Hz for all azimuth active scan angles up to 10° minimum of 75% with a maximum scan angle of 5.5° when using 30 Hz low power board

(f) Scan jitter in azimuth: 0.75 milliradian maximum in the scan direction

(g) Scan jitter in interlace: interlace repeatable with ±10% deviation of height of a display element over center 80% of azimuth field of view; maximum average interlace displacement ±15% of initial setup at 25°C over specified operating temperature range; after soaking at -62°C, interlace will return to within 15% of initial setup when stabilized at -30°C.

(h) Phase shift: design includes provisions for adding a phase shift lens for optical compensation of phase shift introduced by video electronics; phase shift lens mounting capability is provided for lenses to compensate for all resolution frequencies up to 40 kHz, with residual total phase shift of less than 25% of one detector subtense at the system display.

(i) Azimuth angular travel: permits adjustment of azimuth angular travel (10° maximum) for unique system requirements; adjustment does not require special tools; adjustments will not reduce scan efficiency below 70% for the bidirectional mode.

(j) Modulation transfer function (MTF): MTF greater than 95% at 0.667 cycles/milliradian when measured in the 30/60 and 60/120 scan rate modes.

(k) Audible noise: at a distance of 25 feet against a quiet noise background in the 30 Hz, low power configuration, noise level shall not exceed maximum sound pressure level as follows:

Center frequency (Hz)	Octave band (Hz)	Maximum sound pressure level (dB) dB: referenced to 0.0002 microbar
125	87-175	40
250	175-350	39
500	350-700	34
1000	700-1400	26
2000	1400-2800	20
4000	2800-5600	20
8000	5600-11200	17

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 TRANSDUCER ALIGNMENT

The alignment of the transducers has been established by the manufacturer and should not be changed or readjusted during the life of the scanner.

4.1.1 TRANSDUCER BRIDGE ELECTRICAL ALIGNMENT

1 - Lock mirror at neutral (both axes).
2 - Apply 2.00 volts DC between terminals 3 and 4.
3 - Connect DC millivolt meter between terminals 5 and 6.
4 - Adjust R3 for min. voltage on meter $<$ .001 volts.
5 - Connect DC millivoltmeter between terminals 7 and 8.
6 - Adjust R6 for min. voltage on meter ($<$ .001 volts).
7 - Disconnect power sources and meter.

4.2 MAINTENANCE CONSIDERATIONS

Preventive maintenance should be performed in an enclosed clean area isolated from sources of contaimination such as chips, oil, oil vapors, dust, etc. Maintenance techniques are those used for precision optical instruments. Use clean, lint-free gloves to prevent placing finger prints or other residue on optical elements. If necessary, the mirror surfaces shall be cleaned with alcohol and clean tissue. Avoid excessive pressure or prolonged rubbing which could damage the optical coatings.

Dust and dirt on optical baffles, printed wiring boards, pivot points, connector contacts, and other electromechanical components should be removed with a non-shedding, soft bristle brush in conjunction with a low pressure, dry air jet. The frequency of preventive maintenance cleaning is a function of the integrity of the housing enclosure and should be determined by operating experience. It is recommended that, initially, cleaning be performed after every 100 hours of operation until experience dictates otherwise. In addition to cleaning, the Scanner assembly should be visually inspected for loose hardware, marred surfaces and finishes, damaged insulation, unusual

wear points, etc., during preventive maintenance.

The flex pivots which support the scan mirror assembly and the interlace gimbal assembly should be changed every 1000 hours of operation during preventive maintenance.

Both the scan mirror and interlace gimbal assemblies are initially balanced by the manufacturer. If maintenance requires replacement of parts on either of these assemblies, rebalancing will be required. Using special fixtures, the balance should be reestablished to attain .015 oz-in. for the mirror assembly and knife edge balance about the interlace axis of the gimbal assembly.

The mirror scan angle is determined by the location of 4 spring assemblies which the mirror arms strike at the extremes of angular travel. The maximum scan angle is 10° for the 60 Hz unit and 5.5 degrees for the low power unit. The location of the 4 spring assemblies can be varied by loosening a clamp screw and positioning the springs to give the required angle of travel. The low power scanner has additionally, elastomer bumpers on the springs to reduce acoustic noise level during operation. These bumpers should be changed after 1000 hours of operation.

As the Scanner Module is common to many system applications, a phase shift lens, when used, must be considered in balancing the gimbal assembly after any maintenance operation or repair to the gimbal and/or its components. A phase shift lens or an identical dummy weight as used in the system application of the scanner being repaired must be installed to the gimbal assembly when balancing. Care must be taken to make sure the phase shift lens or its dummy weight is properly seated as it will be installed in the final assembly of the scanner module.

CHAPTER 12

DETECTOR/DEWAR INFRARED

USAECOM SM-D-773781

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Detector/Dewar, Infrared module hereinafter called the detector transduces the infrared energy incident upon it, into electrical signals which are a video representation of the infrared scene. The detector contains 180 detector elements in a linear spaced array having separations equal to the detector size, thus permitting 2:1 interlace when used in a Forward Looking Infrared (FLIR) or Thermal Imaging System.

1.2 INTENDED USE OF ITEM

The detector has been designed to be interfaced with other major common and special modules to form an integrated FLIR or Thermal Imaging System. The function of the detector is to transduce the infrared energy from the target scene into video signals. This infrared energy would normally be focussed on the detector array by the IR Imager module after scanning by the mechanical scanner. There are 180 detector elements of which all or a fraction may be used in any given FLIR. Normally, the number of elements used would be selected in groups of 20 since each preamplifier modules provides 20 channels. The video outputs of the detector are fed to the preamplifier for amplification and processing. The number of detector elements used will depend upon the number of channels required by the system being designed.

1.3 TECHNICAL SPECIFICATIONS

The technical specifications of the detector are as follows:

Parameter	Specifications
Material	Mercury Cadinium Telluride
D* 162 element	$\geq 2.4 \times 10^{10}$ CMHz$^{1/2}$ watt $^{-1}$

Parameter		Specifications
	171 elements	$\geq 1.6 \times 10^{10}$ CM $Hz^{1/2}$ $watt^{-1}$ (no detective elements among central 36 elements)
Time Constant		≤ 5 microseconds.
Operating Temperature		80°K +5°, -20°
Responsivity	(95% of element)	$\geq 1.1 \times 10^{4}$ volts/watt
	(average)	$\geq 1.4 \times 10^{4}$ volts/watt
Bias Power	(total -180 elements)	$\leq$ 50 milliwatts
Bias Current	(Maximum)	6 milliamperes
	(average)	$\leq$ 3 milliamperes
Spectral Response		7.5 to 12 micronmeters.

NOTE

For interface information such as mechanical configuration, outline dimensions, electrical interconnection and mounting information, refer to Section III.

SECTION II

FUNCTIONAL DESCRIPTION

2.1 GENERAL

The detector is composed of 180 elements of photoconductive Mercury Cadmium Telluride (Hg CdTe). The detector bias resistors are an integral part of the detector module. Bias current is supplied by the bias regular module. The detector operates by converting incident infrared energy to electrical video signals using the photoconductivity process.

The detector has no controls or adjustments, and is directly interchangeable with other detector modules.

2.2 THEORY OF OPERATION

2.2.1 PHOTOCONDUCTIVITY

Photoconductivity is a characteristic of certain materials wherein radiation is converted to an electrical signal. The electrical signal is manifest as a change in the resistance of the detector material generally producing a change in voltage across the detector element being supplied with a constant bias current. Photoconductors fall into the class of detectors known as quantum detectors. A quantum detector is one which absorbs light quantum directly applying the energy to making an electron available for the conduction process. All semiconductors are characterized by having a conduction band, a path which is partly filled with electrons and which is entirely responsible for the resistance of the material. They also have a valence band which is filled with electrons but cannot contribute to the conductivity. Electrons can be "pushed" from the available sink of the valence band to the conduction band by the addition of energy to the material. This energy can

take the form of radiation (photons) or heat (phonons). The "band gap" of the material is the energy which must be supplied to a valence band electron to push it into the conduction band where it can actively take part in material conduction lowering its resistivity. The length of time which the electron remains in the conduction band before returning to the valence band (with the subsequent release of bandgap energy in the form of heat) is a characteristic of the material and results in its "time constant."

All the energy of a photon is generally applied to only one valence band electron; and each valence band electron can only be acted on by one photon at a time. Therefore, radiation of wavelength lower in energy than the material bandgap will be unable to excite the material to photo conductivity. Since the longer the wavelength the lower the photon energy, the detector material with its characteristic bandgap will determine the longest wavelength which can be detected by a detector constructed of the material. There is no upper limit short wavelength cut off for a photoconductor; and indeed some infrared detectors are used as X-ray detectors; however, as radiation wavelength decreases, energy is "wasted" in that more is available per photon than is needed to excite a valence band electron to the conduction band, so more watts for short wavelength radiation will be needed to produce the same conduction band electron density, a "signal" from a detector element than would be required to elicit the same signal from radiation, with wavelength at the material cut-off. For this reason, a detector is most efficient when operated at its wavelength cut-off than at any other wavelength.

Detector material choice is usually determined by the wavelength of the radiation to be detected. Since the common module is designed to detect radi-

ation is the 7.5-12 micron band, a material with bandgap corresponding to 12 micron radiation is both most efficient and necessary. Alloys of HgCdTe have been synthesized which possess this bandgap (0.1 eV equivalent to 12 micron photon energy).

A major operating constraint on any photoconductor sensitive to 12 micron photons is the phonon competition. As previously mentioned, an alternative way to generate carriers is through phonon energy, i.e., thermal energy. At room temperature (27°C, 300°K) there is for more phonon energy available to the detector than is typically available from the radiation. Therefore, this thermal energy is in parallel with the radiation energy and swamps out of the effects of the radiation energy reducing the sensitivity of the detector element. Simply, so many electrons are thermally excited to the conduction band at room temperature that those excited by the radiation are "lost in the shuffle." To overcome this problem, the detector element must be cooled. The colder it is, the more sensitive it will be to radiation. However, for 12 micron HgCdTe, operating temperatures below 100°K are generally sufficient to produce conduction band electrons at the radiation level, present in common module applications where there is a 300°K radiation background. For this reason, the detector element must be cooled to such operating temperature before they will exhibit radiation sensitivity.

2.2.2 GENERAL CHARACTERISTICS OF HgCdTe DETECTORS

$Hg_{(1-x)} Cd_x Te$ alloys with $X \approx 0.2$ are semiconductors with a bandgap of approximately 0.1 electron volts at 80°K. For this reason, this material is ideal for the fabrication of photoconductors sensitive to radiation with photon energy at the higher than 0.1 eV which corresponds to 12 microns.

At 80°K, HgCdTe detectors generally exhibit nominal resistance of 50 ohms/square. However, there are several complex interactions which relate device resistance, time constant responsivity and D* to temperature.

2.2.2.1 Temperature Effects

Band gap of HgCdTe, unlike most semiconductors, increases with increasing temperature, hence a nominal operating temperature below 100°K is necessary for the element to be sensitive to 12 micron photons. As temperature decreases, the number of thermal electrons in the conduction band decreases which results in a lower conductivity condition from this source. However, the mobility of the conduction band electrons increases as temperature is lowered in certain ranges. Since element resistance is a function of the product of number of electrons times then mobility, the temperature dependence of these two effects tend to cancel each other, producing a leveling of element resistance. Element resistance is not a strong function of temperature, and is definitely nonlinear with respect to temperature. Figure 2-1 shows a typical resistance vs. temperature characteristic.

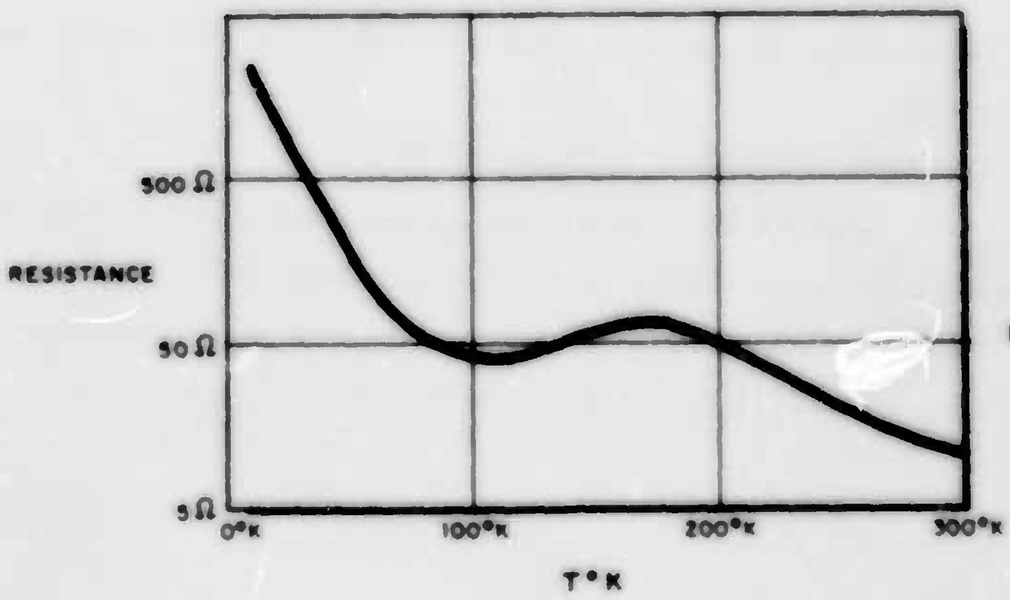
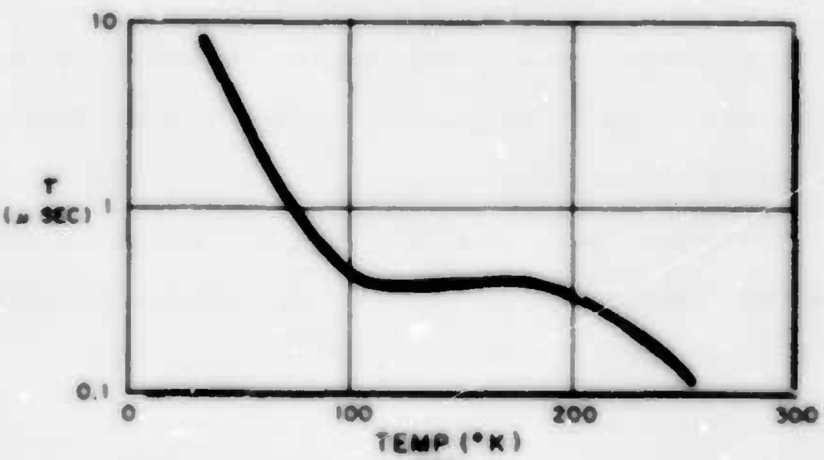


Figure 2-1

Time constant is also a complex function of temperature. In the absence of trapping effects, time constant is independent of temperature. However, all semiconductors have "traps" which trap an election or a hole and make it unavailable for "recombination." When an electron leaves the valence band,' it leaves a hole behind, if the hole becomes "trapped", it will be unavailable for electron recombination and the electron will be unable to return to the valence band for the duration of the time that the hole is trapped. Electron traps in the conduction band also exist, and they not only make the electron unavailable for recombination, but also prevent its taking part in the conduction process. Therefore, hole traps increase the response time. Electron traps increase response time and reduce sensitivity.

As temperature decreases, there are fewer "background" electrons and holes, hence more traps available to "catch" them. The number of traps, however, are a function of bandgap which is also temperature dependent. Electron traps do not generally have a significant effect on device time constant, however, hole traps have a large effect. Below 100°K, time constant generally increases with decreasing temperature. Between 100-140°K, time constant generally levels off with temperature as the increasing number of thermal corners is offset by the additional traps being exposed as bandgap opens. Above 140°K, time constant decreases with increasing temperature. See figure 2-2, below.



2.2.2.2 Responsivity vs. Temperature

Responsivity is a direct function of resistance and a direct function of time constant. As temperature is adjusted in the 80°K to 100°K range, there is little effect due to temperature change. However, at very low temperature, responsivity will increase dramatically and at high temperature it will decline.

2.2.4 DETECTIVITY VS. TEMPERATURE

Detectivity is a function of responsivity and noise is a function of both resistance and temperature to the one-half power. Since noise is directly related to temperature if responsivity is constant over a given temperature range, with resistance also constant over the same range, as is typical of these devices detectivity will decrease with increasing temperature at the one-half power rate.

2.3.2.3 Bias

In order to collect and measure the electrons which result from the incident radiation, an electron field must be applied to the device in the form of a voltage. Since the device has a quiescent resistance, a current, the bias current, will flow with the application of the bias field. There are several effects which combine to determine an optimum bias for each detector.

As bias is increased, the photogenerated carriers feel an increased field and are more vigorously collected. Therefore, in the absence of other effects, responsivity and D* will both increase with increasing bias. However, as bias is increased, thermal loading increases due to I^2R dissipation in the device. At some point this electrical or bias heat input will exceed the capacity of the cooling system, and the detector will begin to increase in temperature with a resultant decrease in D*.

Time constant of the detector is usually determined by the average time an electron requires to recombine with its corresponding hole in the valence band. However, when the bias field is sufficiently intense, these carriers may be "swept out" of the detector before recombining. This is known as the "sweep out mode" of operation. It results in a bias controlled response time and maximum possible D* which are both desireable characteristics. A bias would normally be chosen which would result in "sweep out" operation. However, if the detector is physically too large, detector heating and loss of D*, will oc occur before reaching the sweep out condition. See Figure 2-3.

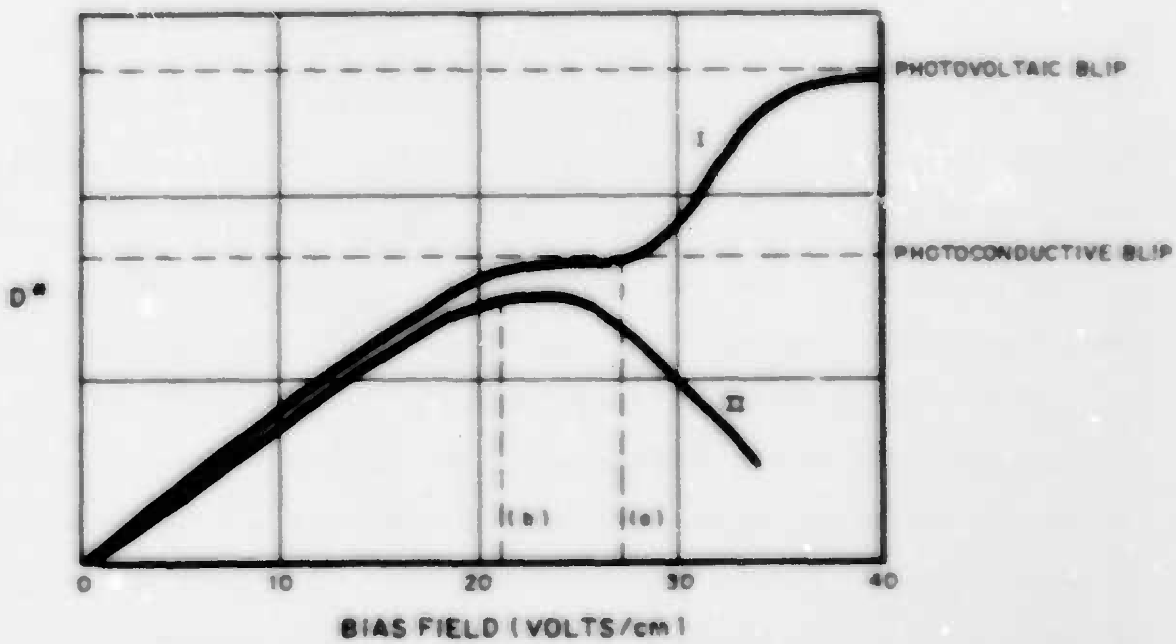


Figure 2-3.

Curve I shows D* vs bias for a detector sufficiently small that it shows the transistion to sweep out mode at bias field (a). Curve II shows D* is bias for a detecter which is too large to dissipate bias heating such that bias is restricted to fields below those resulting in sweep out. In this case the device would normally be operated a bias field (b).

Other considerations which have an effect on bias choice include preamplifier noise and environmental noise contributions. Since such noise contribution are generally constant, overall system signal to noise performance might be increased by operating at a bias higher than optimum for the detector alone to increase responsivity so that more signal is available to overcome system noise effects. Generally, best system performance for any given detecter is obtained when bias is adjusted so that detector noise is the dominant noise contribution.

2.2.2.4 <u>Other Characteristics</u>

When a detector is presented with a signal source which is a uniform gray surface at a given temperature, the arrival of photons is non-uniform. There is a random fluctuation in the rate of photon emmission from the surface. When the detector is sufficiently sensitive to detect these fluctuations, they appear as "Noise", and the detector is said to be background limited. Further increasing sensitivity will also correspondingly increase the output responding to the background fluctuations, so signal to noise will remain constant.

In an effect to further increase detector performance, it is sometimes "cold shielded" so that it will see less of this background radiation, and hence less fluctuation signal. This procedure results in a noise decrease and a corresponding D* increase, however, it also results in a numerically higher f/number which correspondingly reduces system resolution. Convenient sizes for optical elements generally set the limit for the amount of cold shielding employed in a given application.

Another way to reduce background noise is to reduce background temperature. This is not often under the control of the system user. Detector performance is optimized for a "room temperature", a 300°K background. If the background

is substantially colder, background noise from the detector will be lower, and system performance might benefit from higher bias settings (to restore detector noise as the major contribution). Conversly, in a high temperature ambient, a lower bias could result in improved system performance. However, a higher than normal ambient will always degrade system performance.

HgCdTe detector are low impedance devices, with resistance generally less than 100 Ω. For this reason they are insensitive to electrostatic interference and capacitive effects. However, they are highly sensitive to electromagnetic interference and inductive coupling of the sort found near motors, relays, coils and other magnetic devices. Appropriate shielding and separation should always be maintained.

The detector in the common module is made of several discrete elements, each simultaneously observing a different part of the scene. It is essential that each detector output remain independent of all others. The inherent low impedance of the devices greatly aids is maintaining a minimum of element to element "cross talk".

SECTION III

INTERFACE

3.1 CONFIGURATION

Figures 3-1 and 3-2 show the pertinent outline and mounting data for use of the designer in incorporating the detector in a system layout. Figure 3-3 is a photograph of the detector module. Also shown in this photograph is the closed cycle cooler.

3.2 DETECTOR CHARACTERISTICS

3.2.1 INPUT CHARACTERISTICS

(a) Detector array: responds to incident infrared radiation in the 7.5 to 12 micrometer spectral region emanating from the target area

(b) Detectivity: peak detectivities normalized to unity bandwidth shall be as follows:
(1) At least 162 elements $\geq 2.4 \times 10^{10}$ CM Hz 1/2 watts^{-1}
(2) At least 171 elements $\geq 1.6 \times 10^{10}$ CM Hz 1/2 watts^{-1}
(3) 9 elements may be less than 1.6×10^{10} CM Hz 1/2 watts^{-1}; no defective elements in center 36 elements of array; defective elements separated by at least one acceptable detector elements.

NOTE:

Peak detectivities are determined from normalized spectral response and blackbody detectivities D^*_{BB} (500, 340, 25 to 35 kHz); noise bandwidth used will reflect the measured test condition in use at time of test; measurements will be made of a 75 degree effective field of view, a 300°K background, and a detector temperature of 80 +5, -20°K)

(c) Spectral response: elements operate in the 7.5 to 12 micrometer spectral region; each element has a spectral cut-off between 11.5 and 12.0 micrometers

(d) Bias power: To meet uniform responsivity, total bias power needed for entire array = 50 milliwatts maximum; average bias current of elements = 3 milliamperes maximum; no one element requires a bias current of more than 6 milliamperes

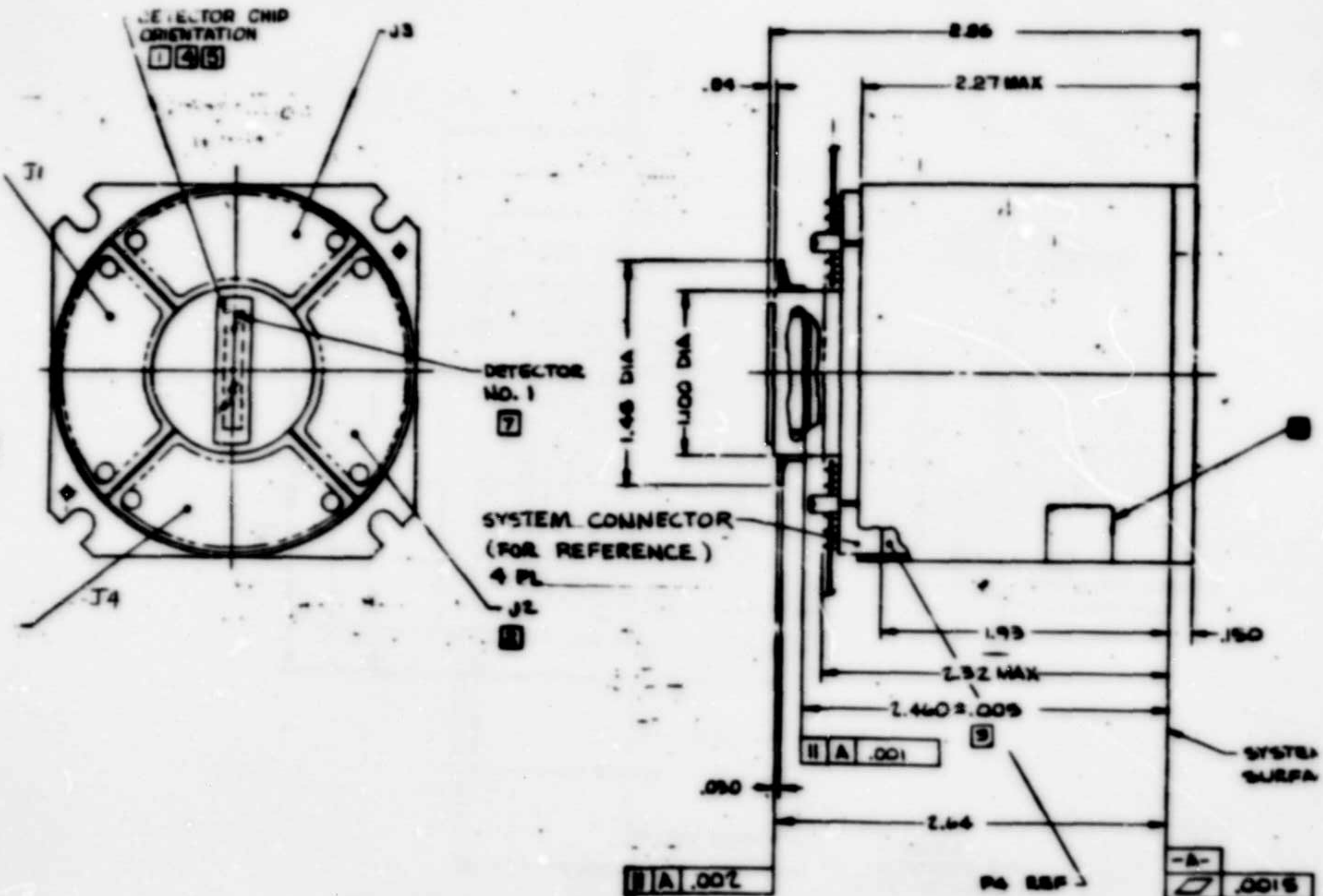


Figure 3-1. Outline Drawing (Sheet 1 of 2)

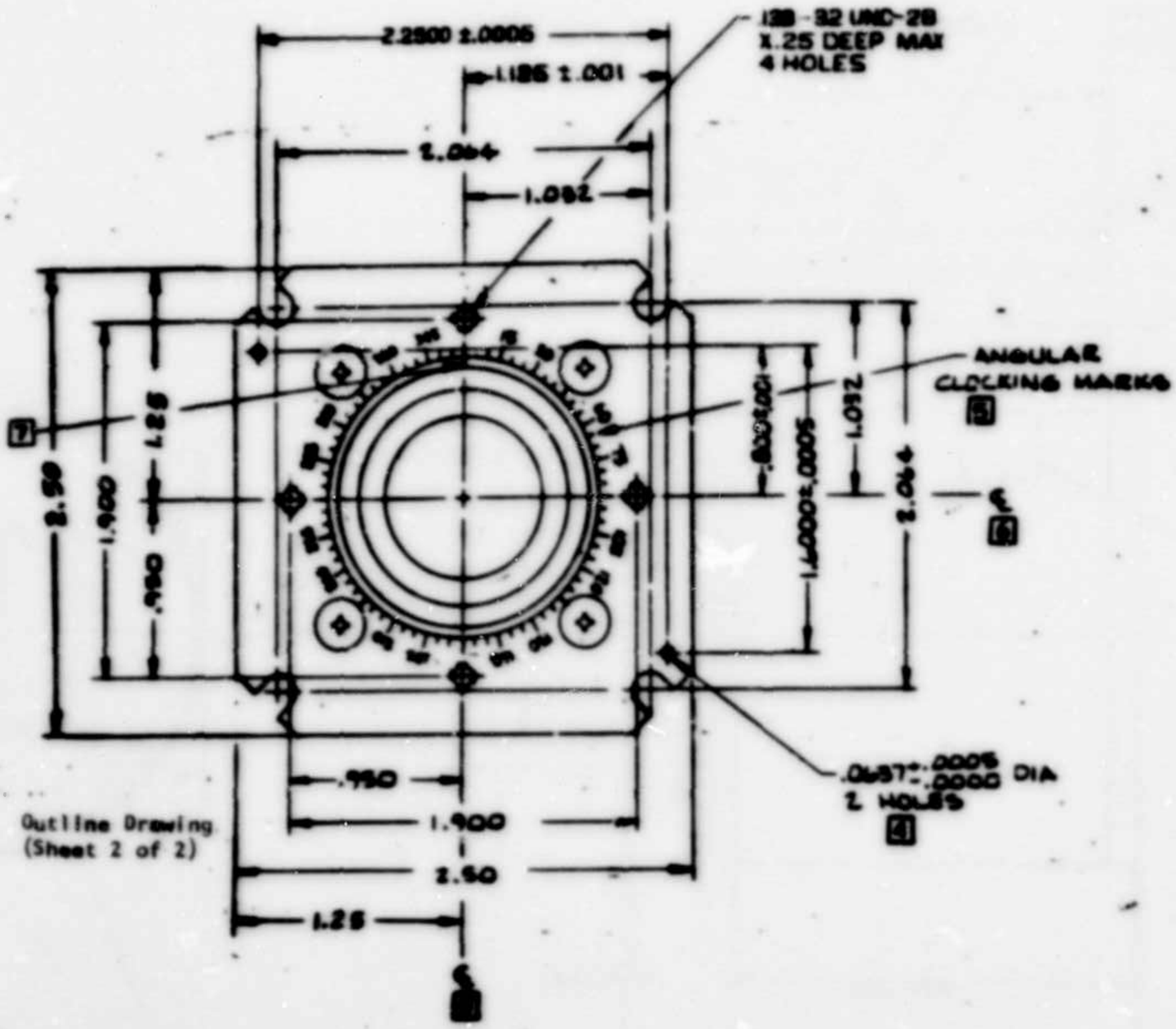
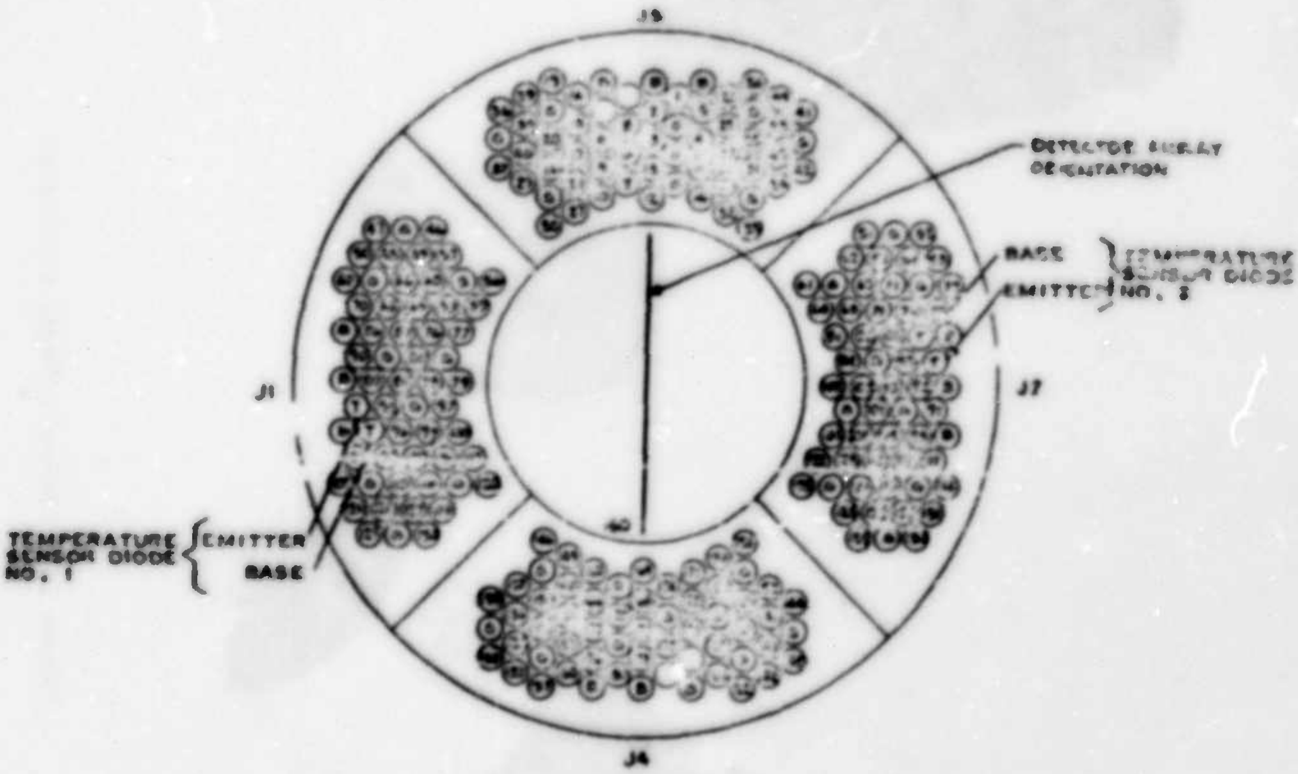


Figure 3-1. Outline Drawing (Sheet 2 of 2)



CONNECTOR PIN PATTERN AS VIEWED FROM DETECTOR END OF DEWAR WITH CORRESPONDING DETECTOR NO'S

Figure 3-2. Connector Pin Pattern

Figure 3-3. Detector/Dewar and Cooler

(e) Dewar window: bandpass filter with 50% transmission wavelengths of 7.5, +0.25, -0.05 and 12.0, +0, -0.25 micrometers; average transmission in band > 85%

3.2.2 OUTPUT CHARACTERISTICS

(a) Electrical connections: one lead from each detector element; minimum of 2 leads for a calibrated temperature sensor

(b) Temperature sensor: minimum of 2 calibrated temperature sensors installed at or near detector location in Dewar provides electrical signal which is an analog of temperature

3.2.3 PROCESSING CHARACTERISTICS

(a) Time constant: less than 5 microseconds when operated at 80 +5, -20°K and a 75° effective field of view (Definition: time constant = time required for detector element response to reach 63% of its steady state value after being irradiated by a step input from a source of 7.5 to 12 micrometer radiation.)

(b) Sensitive area: sensitive area of detector elements, define as the 50% voltage line response of the elements, will conform to dimensions in figure / entitled; "Detector element size and spacing". See B2 specification.

(c) Crosstalk: signal from a non-irradiated detector will not exceed the noise level of a typical detector element by more than 40% under following conditions:

(1) Any other element irradiated by a 7.5 to 12 micrometer source
(2) Signal-to-noise ratio from radiation source is ≈ 20:1
(3) Image of source ≤ geometrical size of detector
(4) detector operating at 80 +5, -20°K

(d) Detector resistance: variation in resistance between elements (less unacceptable elements) will not exceed 40% of the mean at 80° +5, -20°K.

(e) Responsivity: peak spectral responsivity of 95% of elements will be ≥ 1.1 x 10^4 volts/watt; average peak responsivity will be ≥ 1.4 x 10^4 volts/watt; uniformity variation will be < 40% of mean value

(f) Operating temperature: 80 +5, -20°K

(g) Cold shield: will limit the field of view of the detector array to an equivalent 75° cone; an external cold shield can be mounted on the Dewar

(h) Heat load: does not exceed 0.4 watt when all 180 detector elements are cooled to 80 +5, -20°K and are operating at their final bias current; heat load to cryostat 370 milliwatts maximum, with center 60 elements operating at their final bias

(i) Vacuum life: Sufficient vacuum will be maintained in Dewar for 1 year with no getter firings or other means of maintaining vacuum with operating or storage temperature or both $\leq$ +71°C; proper vacuum will prevent the front windows from frosting when operated or stored under specified conditions

(j) Getters: Minimum of 2 reusable, electrically activated getters, which can be activated at least 7 times are provided

(k) Detector orientation: array orientation with respect to Dewar mounting flange variable through 360 degrees; orientation indicated by reference mark on base plate designating detector No. 1; orientation of detector with respect to clocking marks on Dewar base within ±1 degree.

NOTE:

Results in tolerance buildup of ±2 degrees from detector array to clocking marks)

3.2.4 ANCILLARY ELECTRICAL DESIGN CONSIDERATIONS

(1) Due to the low level signal outputs of the detector element and their subsequent high amplification by the Preamplifier/Control Driver, the detector element signal output leads should be isolated from any other signal source to avoid crosstalk and/or extraneous pick-up.

(2) Detector element signal output leads to the preamplifier should be kept as short as possible.

3.2.5 DETECTOR COOL DOWN MEASUREMENT.

Two diodes within the detector module permit measuring the temperature achieved at the detector array. Since the forward bias voltage drop across a diode varies with temperature, the temperature of the detector array can be determined by measuring the voltage drop. A typical diode voltage versus temperature chart for the detector is shown in Figure 3-4.

3.4 BASIC OPERATING PRECAUTIONS

(1) Connection from the detector should only be made when there is known to be zero volts on the leads making the connection.

(2) Coupling capacitors must be fully discharged before connection to the detector. Failure to observe this precaution may lead to detector burn-out.

(3) Bias field should be applied only through appropriate load resistors, and only after connection of the detector to amplifier inputs and coupling capacitor.

(4) Continuity should never be checked with a standard ohmmeter as currents produced by such instruments generally far exceed those tolerable by the detector possibly resulting in burnout.

(5) Maximum bias current which should ever be presented to any detector element under any circumstance is determined by the expression I (in milliamperes) = 200/R (element resistance in ohms).

(6) So long as bias current is limited to the conditions of (5) above, it can be applied at any operating temperature.

(7) Leads and interconnections.

(a) Leads must be dressed to minimize crosstalk

(b) Due to the low impedance of the device, it is essential that leads not be placed in such a way to allow high inductive currents to build. It is possible to produce destructively high currents in detector circuits through magnetic inductive coupling to strong field devices such as unshield transformers or motors.

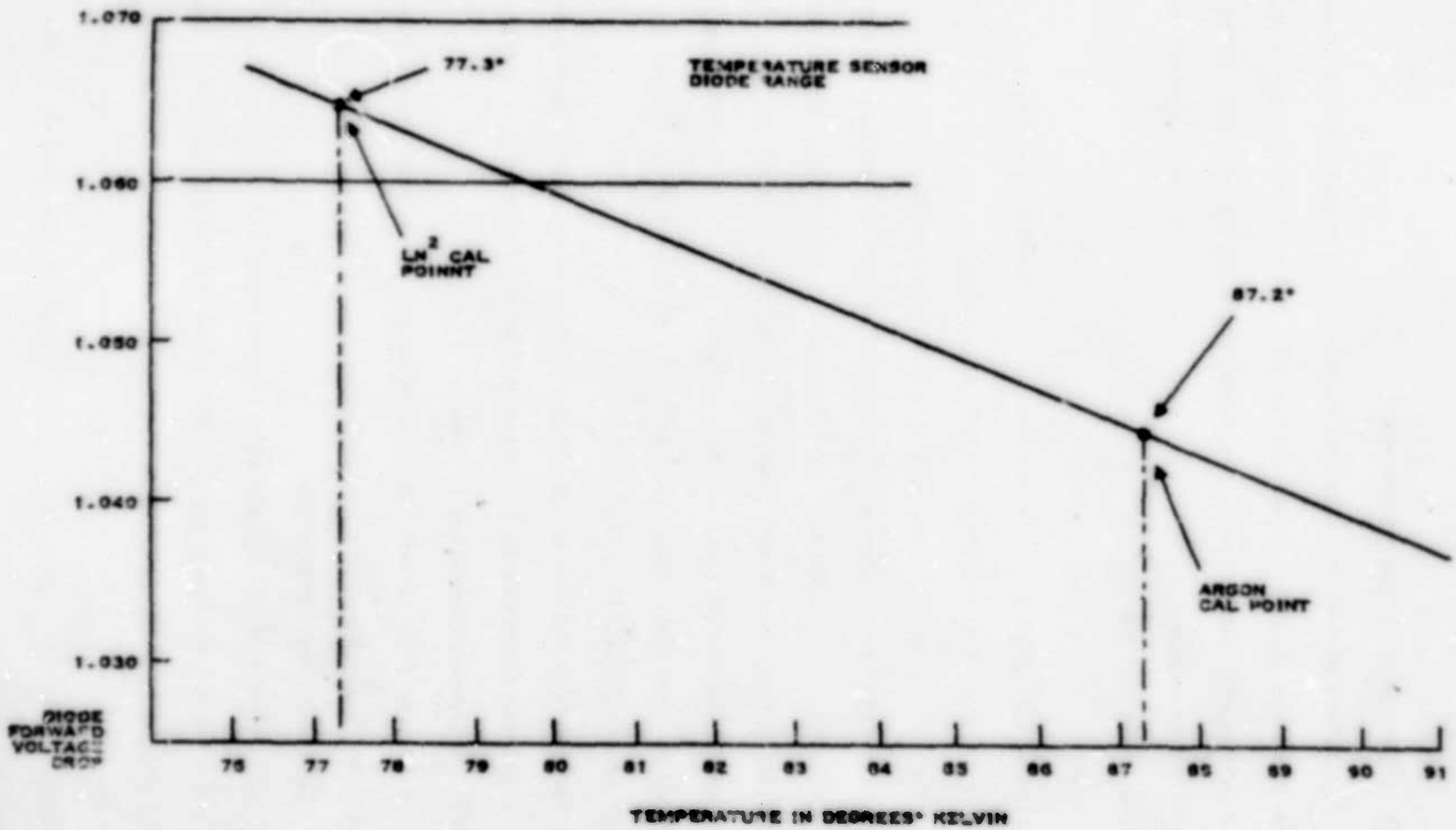


Figure 3-4. Detector Diode Temperature Sensing Chart

(c) Never store detector in shorted condition.

(8) Be sure that the detector dewar bore is absolutely free of moisture for assembling to the cooler.

(9) Window and housing parts may crack or break if subjected to high impact. Always transport detector in the container in which it was shipped until installation in FLIR.

3.3 INTERCONNECTION INFORMATION

The detector/dewar must be provided with a means of cooling the detector to a temperature of about 77°K. Although the common modules cooler shown in Figure 3-3 is considered the normal means of providing this cooling, other devices may be used. Another form of closed cycle cooler has its cold finger separate from the compressor, but connected to it by a length of small high pressure tubing up to about two feet long. This permits greater freedom in locating and mounting the module. Either of these types can operate with the cold finger in any attitude. For static operation where the dewar can be mounted facing downward, liquid nitrogen may be used as the cooling medium by simply pouring it into the dewar. A different liquid nitrogen system which permits the dewar to be mounted horizontally or even tilted slightly upward, involves use of a slightly pressurized liquid storage dewar and a control system which feeds the liquid as droplets through a small tube to the end of the detector-dewar. There the liquid is caught and held by a small mat of fibres until it evaporates. Compressed dry nitrogen or air may also be used in a Joule-Thompson cryostat to provide cooling. This too can be mounted horizontally like the previous type. If the size of the cold finger or cryostat is not a direct equivalent of that shown in Figure 3-3, a special adapter may be needed to mate with the detector-dewar.

3.4 INSTALLATION INSTRUCTIONS (See Figure 3-5)

This procedure establishes a method of installing and removing the Detector Dewar on the Cooler.. To prevent damage to the Dewar and to establish a good thermal bond between the Cooler and Detector.

PARTS REQUIRED

1 Cooler (SM-D-773683)
1 Detector/Dewar (SM-D-773780)
1 Bellows (SM-C-772797)
1 O-Ring (SM-C-773504-4)
AR R.T.V Adhesive (SM-C-773480-1) Dow Corning Silastic 732 RTV
AR Thermal Compound (SM-C-773551) Wakefield Engineering Type 120
4 Screws - #6-32 x 1/2 S.H. (MS16995-18)
4 Split Washers - #6 (MS35338-136)
1 Allen Wrench, 7/64, with 1/4" length right angle
AR Flat Washer #6 (AN960C-61) See installation step 5
AR Flat Washer #6 (AN960C-6)

Caution

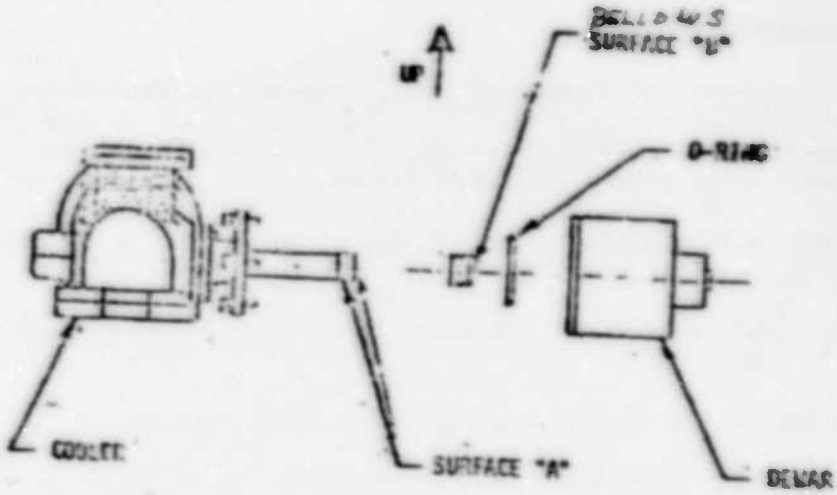
Use extreme care in handling the Cooler and Dewar. The cold finger is very thin metal and the dewar is glass.

1. Check that bellows will fit on the end of the cooler cold finger.

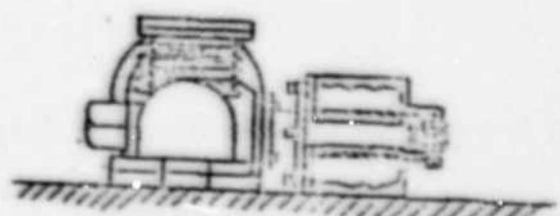
2. Coat cooler cold finger surface "A" with a thin coat of thermal compound.

3. Fill the front two convolutions of the bellows with thermal compound to a level just past the vent hole.

4. Coat bellows surface "B" with a thin coat of thermal compound.



A



COOLER-DETECTOR ASSEMBLY

B

Figure 3-5 Installation

MODULAR COOLER/DETECTOR-DEWAR ASSEMBLY

DEWAR INSTALLATION (CONT.)

5. Insert four (4) screws with split washers in small holes of cooler cold finger flange. Caution: The screws must extend $.25 ^{+.00}_{-.03}$ into the detector/Cooler module. Select flat washers and place between lock washers and cooler flange to control screw projection.

6. Apply R.T.V. adhesive to o-ring and install o-ring in groove of dewar.

7. Set cooler (head up) and dewar (0° up) on a flat surface as shown in Figure 3-5.

8. Place the bellows on the end of the cold finger.

9. Carefully slide dewar onto end of cooler cold finger until the bellows touches the bottom of the dewar recess.

10. Slowly move the dewar farther onto the cold finger until the dewar is in contact with the flange on the cold finger.

11. Start the two side screws and evenly snug them up to the o-ring by hand.

12. Tighten the two side screws by turning 1/4 turn in sequence until flanges meet. Observe gap during tightening and maintain parallelism.

13. Insert top and bottom screws and tighten.

14. In sequence check all screws for tightness.

DEWAR REMOVAL

Caution

Use extreme care in steps 4 through 7 so as not to damage the dewar and cold finger.

1. Detector must be at room temperature before removal. If in doubt, allow two (2) hours non-operating before proceeding.

2. Remove top and bottom screws.

3. Set cooler-dewar (head up) on a flat surface as shown in Figure 3-5.

4. Remove side screws by turning each 1/4 turn in sequence.

5. Gently rotate to break R.T.V adhesive on o-ring.

6. Withdraw dewar off the cold finger.

7. Remove bellows from dewar stem.

SCOPE

This procedure establishes a method of assembly for the Modular Cooler-Detector to prevent damage to the Dewar and to establish a good thermal bond between the Cooler and Detector.

PARTS REQUIRED

1 Cooler (P/N) 799901-1)
1 Dewar Detector (P/N 799899-1)
1 Spring (P/N 419346-140-1)
1 Cold Plug (P/N 833344-1)
1 O-Ring (P/N 537531-123)

AR R.T.V. Adhesive (P/N 412814-4) Dow Corning Silastic 732 RTV

AR Thermal Compound (P/N 415886-1) Wakefield Engineering Type 120

4 Screws - #6-32 x 1/2 S.H. (P/N 418262-18)

4 Split-washers - #6 (P/N 418262-18)

1 Allen Wrench, 7/64, with 1/4" length right angle

DEWAR INSTALLATION

1. Check that cold plug will slide smoothly over cooler cold finger.
2. Coat cooler cold finger surface "A" with a thin coat of thermal compound.
3. Coat cold plug surface "G" with a thin coat of thermal compound.
4. Insert Cold plut into dewar stem and seat it against the bottom of the stem as shown.
5. Insert four (4) scews with split washers in small holes of cooler cold finger flange.
6. Adhere spring to center end of cooler cold finger with thermal compound.
7. Apply R.T.V. adhesive to o-ring and install o-ring in groove of dewar.
8. Set cooler (head up) and dewar (0° up) on a flat surface as shown in Figure 2.

9. Carefully slide dewar onto end of the cooler cold finger until the cold finger touches the cold plug.

10. Gently move the dewar around until the cold plug slides onto the cold finger.

11. Start the two side screws and evenly snug them up to the o-ring by hand.

12. Tighten the two side screws by turning 1/4 turn in sequence until flanges meet. Observe gap during tightening and maintain parallelism.

13. Insert top and bottom screws and tighten.

14. In sequence check all screws for tightness.

DEWAR REMOVAL

1. Detector must be at room temperature before removal. If in doubt, allow two (2) hours non-operating before proceeding.

2. Remove top and bottom screws.

3. Set cooler-dewar (head up) on a flat surface as shown in Figure 2.

4. Remove side screws by turning each 1/4 turn in sequence.

5. Gently rotate to break R.T.V. adhesive on o-ring.

6. Withdraw dewar off the cold finger.

7. Remove cold plug from dewar stem.

CAUTION

Follow steps 4 and 7 carefully as stem is made of glass.

SECTION IV

TEST/MAINTENANCE

4.1 GENERAL

This section provides information on the test and maintenance requirements to be considered in the use and application of the detector module. Presented herein are the test equipment requirements and the maintenance procedures.

4.2 TEST EQUIPMENT AND TOOLS

The following, or equivalent, test equipment is required to perform the necessary operational tests.

4.2.1 STANDARD TEST EQUIPMENT

Table 4-1, following, presents a listing of commercially available equipment which has been found to be adequate for testing this module.

TABLE 4-1

STANDARD TEST EQUIPMENT

Equipment	Manufacturer	Model
Digital Voltmeter	Fairchild	7000
Metric Scales (0-10 gr)		
Power Supply ±15 Vdc		
Resistor 15.0 ±0.1 K		
Stop Watch		

4.2.2 SPECIAL TEST EQUIPMENT

No special test equipment is required to test the detector

4.2.3 SPECIAL TOOLS

No specials tools are required to test this module.

4.3 TEST PROCEDURE

4.3.1 PURPOSE

The purpose of the detector test is to determine that the detector module meets acceptable requirements before installation into a FLIR. The minimum standards of performance determine the specific requirements that the detector must meet when used in a FLIR.

4.3.2 METHOD

The detector is connected to the test setup as shown in Figure 4-1. All test interconnections are checked. Pin locations are shown in Figure 3-2. The test is performed as specified by test procedure steps listed in table 4-2. Each test is performed in the sequence shown. Each step of the sequence, when performed verified against the performance standard listed in the right hand column of Table 4-2.

4.4 MAINTENANCE PROCEDURES

Each module is cleaned during maintenance, and after 100 hours of operation, or more often if necessary. Cleaning materials and protective agents are listed in Table 4-3. Where the use of an air jet is specified, use a hand operated air nozzle supplied with clean, dry, compressed air at a pressure of 25 psig maximum.

The connectors are cleaned as follows:

a. Wipe dust and dirt from bodies, shell, coupling nuts, and cable clamps, using a soft-bristled brush.

b. Remove dust from inserts, using a small, soft-bristled brush in conjunction with an air jet.

c. Wash dirt and any trace of lubricant from insert, insulations, and contacts, using a small, soft-bristled brush to apply general purpose cleaner sparingly.

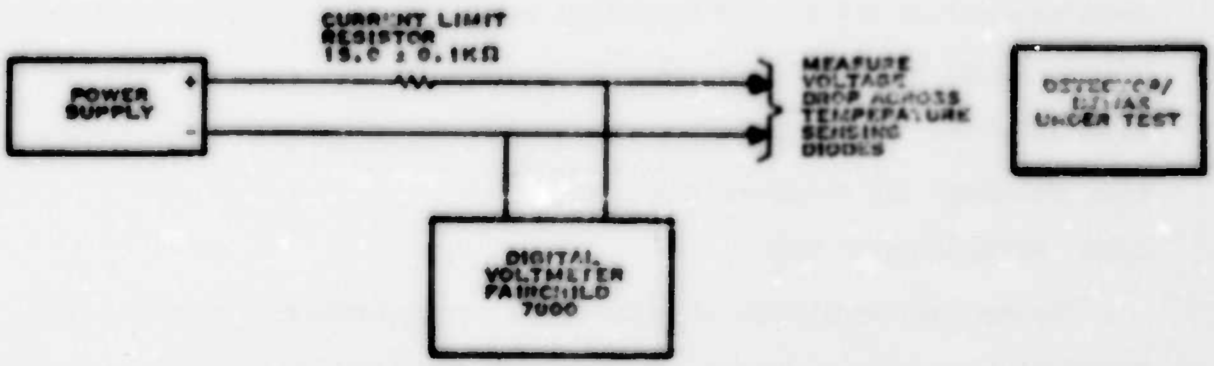


Figure 4-1. Test Set Up

NOTE

Do not allow general purpose cleaner to run into sleeves (or conduit) covering wires or cables connected to contact terminals of the insert.

d. Dry connectors with air jet.

4.5 DETECTOR VACUUM INTEGRITY

4.5.1 SYSTEM DIAGNOSIS

A suspect detector having poor vacuum (and excessive heat loading) cannot be accurately diagnosed while it is mounted to a cooler within a system. Only two measureable operating characteristics are available: detector stem/chip temperature (from I-V data of the 2N2222 transistor) and input power to the cooler. These data cannot be used to diagnose a problem and attribute its cause to either the detector or cooler alone. The detector must be removed from the system and demounted from the cooler.

4.5.2 DETECTOR BENCH TEST

The most accurate means of determining vacuum integrity is by the test described in the B2 development specification B2-28A050102, "Heat Load, paragraph 4.2.5.2.2. A quick determination may be made however by filling the Dewar's bore one-third full with LN_2. A Dewar with normal vacuum and heat load less than 0.400 Watts will allow the LN_2 to evaporate with no noticeable signs of boiling. That is, the surface of the LN_2 is quiescent with no visible bubbles.

4.5.3 GETTER FIRINGS

The specification requires that the getters shall be capable of being fired seven (7) times, although this number may be as many as twenty if a catastrophic vacuum failure has not occurred. The manufacturer usually fires both getters (and also performs the initial bake-out) one time. A typical fir-

ing procedure is to fill the Dewar's well with LN_2 and then immediately fire both getters sequentially at a current of 3.5 Amps, for approximately two minutes. Details of pumping speed and capacity may be found on drawing SM-C-772743.

Table 4-2 Detector/Dewar Module Test Procedure

Step No.	Test Procedure	Performance Standard
	Vacuum Test: The following procedural steps provide a simple straight forward method of determining detector/dewar module vacuum integrity.	
1.	Place the detector/dewar module on the metric scales and adjust for a zero balance.	
2.	Carefully pour liquid nitrogen LN2 into the detector/dewar module stem. Continue pouring the LN2 until the boil off rate stabilizes with a liquid depth of 1/2-inch.	
3.	After an elapsed time of 2 minutes, adjust the LN_2 level to measure 2.5 grams above the scale zero balance, then start stop watch.	
4.	Adjust balance weights down to 2.0 grams.	
5.	Record the time required to boil away 2.0 grams of LN2. Temp Temperature Diode Test: This test determines the reliability of the temperature sensing diodes within the detector/dewar module.	If the LN_2 boil-off rate is less than 0.1 grams/minute then consider the vacuum integrity of the detector/dewar module to be good. Should the boil-off rate exceed 0.1 grams/minute then return the module to factory for repair.
6.	Locate temperature diodes connector pins in the detector dewar connector as shown in Figure 3-2.	
7.	Connect digital voltmeter and power supply with current limiting resistor as shown in Figure 4.1.	
8.	Carefully pour LN_2 into stem of the detector/dewar module, until the boiling rate stabilizes within approximately 1/2-inch liquid depth.	
9.	After 2-minutes has elapsed read the voltage drop across diode #1 by placing the	Voltage drop shall be within 1.060 to 1.070 Vdc if diode

Table 4-2 Detector/Dewar Module Test Procedure (Cont.)

Step No.	Test Procedure	Performance Standard
	test setup positive probe ( ) to the base pin and the other to emitter pin (connector J1, Figure 3-2).	#1 is in good condition (reference Figure 3-4).
10.	Moves test circuit and check diode #2. Use same procedure as step 9.	Voltage shall be within the same range as in step 9.

Table 4-3. Cleaning Materials and Protective Agents

Item	Name	Manufacturer or MIL/FED Spec No.
Solvent	Acetone	JAN-A-489 FED Spec O-T-51C
Cleaners (general purpose)	Methylene Chloride Tetrachlorethylene Solvent, Dry Cleaning Toluene, Technical	MIL-M-6998 FED Spec O-T-236 FED Spec P-D-680 FED Spec TT-T-548
Cleaning solution	Ethyl Alcohol	FED Spec O-E-760b, Grade I, Class A or B
Cloth, Cotton (nonlinting)		FSN 8305-715-8750

CHAPTER 13

LIGHT EMITTING DIODE ARRAY, INFRARED

SM-D-773638

SECTION I

GENERAL DESCRIPTION

1.1 Introduction

The Light Emitting Diode Array, Infrared (LED array) performs the function of converting detected and amplified infrared radiation (video signals) to visible light. This conversion is accomplished by the LED array which is comprised of one multi element light emitting diode array integrated with a set of system connectors. The drive signals applied to the LED array are normalized by internally packaged resistors which provides a normalized (current limited) signal input to the LED array. This permits the LED array to supply constant contrasting visible displays. The visible display emitted by the LED array varies in direct correspondance with the input drive signals supplied by the externally connecting modular system electronics.

1.2 Intended Use of Item

The LED array is positioned in the focal plane of the scanner/visual collimator optic. The collimated light from the LED array is directed to the reverse side of the scanning mirror.

The visual analog of the scanned IR scene will be presented to a viewer observing the scanned LED array. The parameters of the scanned infrared scene such as resolution, contrast, and field of view are faithfully transmitted to the LED array by way of the preamplifier, postamplifier, and LED driver electronics train.

SECTION II

FUNCTIONAL DESCRIPTION

2.1 THEORY OF OPERATION

The light emitting diode is a solid state quantum light emitter rather than a thermal or plasma light source. A diode chip of gallium arsenide phosphide will emit light when the diode is injected with a forward bias current which builds up the junction voltage above a knee which is approximately 1.4 volts. Light output increases with current in a linear fashion, where the diode is biased above the knee voltage.

The internal mechanism of the LED is explained by the various energy bandgaps in a semiconductor. Forward current flow pumps electrons up to the conduction energy band into an unstable state. As electrons from the conduction band fall back into the valance band, they give up energy in recombining with holes. This energy is given up in the form of light. The particular light frequency emitter depends on how far the electrons fall and this distance is related to the energy gap between the valence and conclusion band. The greater this band, the higher energy or high frequency the emitted radiation. The numerical value of the knee voltage is just slightly lower than the numerical value of the bandgap energy in electron volts.

SECTION III

INTERFACE

3.1 CONFIGURATION

Figure 3-1 shows the pertinent outline and mounting data for use of the designer in incorporating the LED Array in a system layout. Note that the dimensions and tolerances reflect the actual drawing data which in some cases differ from or supplement the data in the B2 specification. Figure 3-2 is the physical dimensions of the diodes and Figure 3-3 is a photograph of the LED Array.

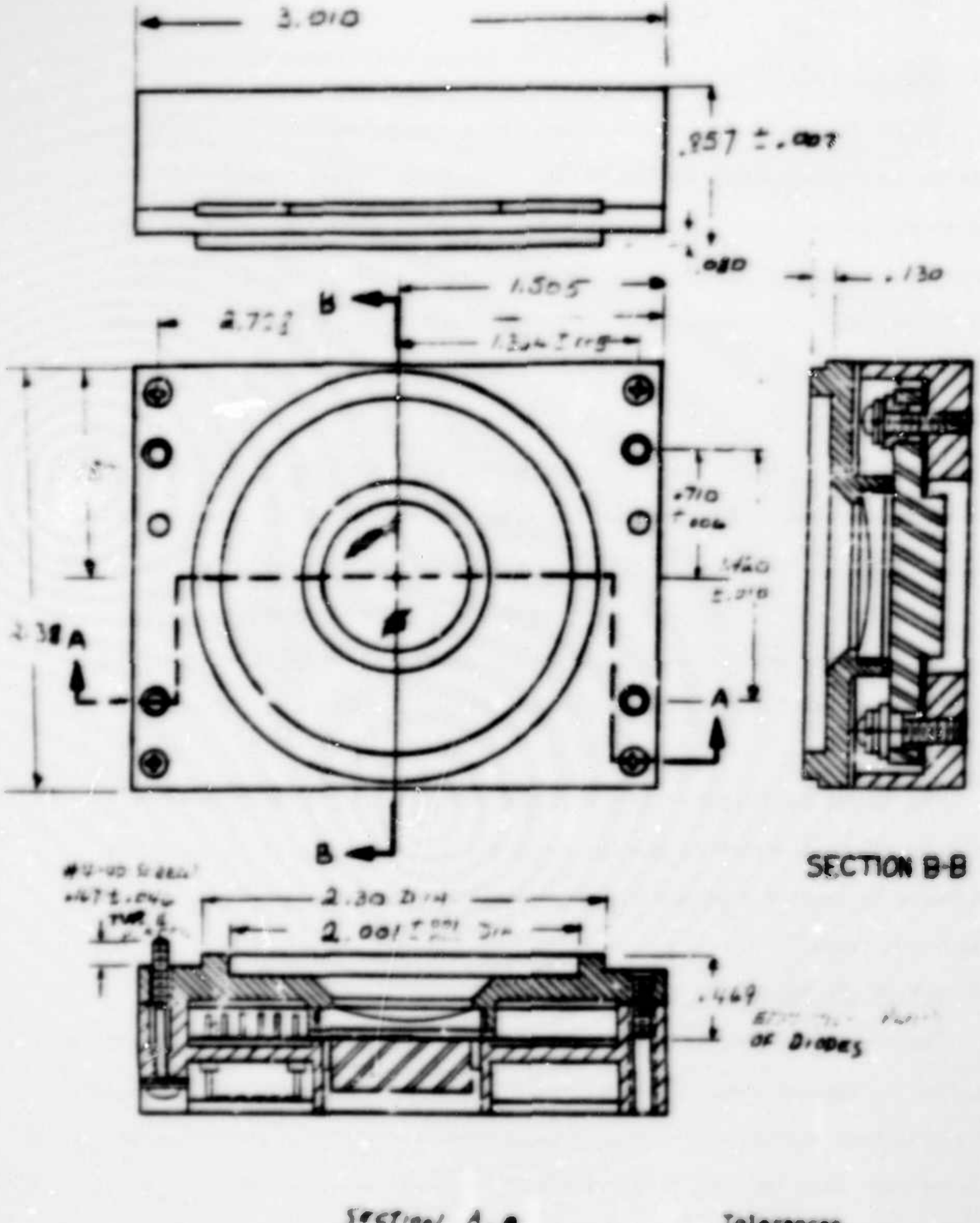
3.2 INTERCONNECTING

The LED Array normally interfaces mechanically with the Visual Collimator and electrically with the Postamplifier/Control Driver module. The number of electrical connections is determined by the number of detector elements used in the system, since each diode corresponds to a detector element. This module can be operated in any attitude, but must be oriented relative to the other optical modules so as to provide the visual output in the required orientation.

The Visual Collimator module does not have mounting holes into which the four mounting screws of the LED Array can be inserted. It is therefore necessary to provide a unique clamping means to attach the LED Array to the Visual Collimator.

3.3 USE OF LED FOR VISUAL DISPLAY OPTICS

The display optics are that portion of the optical system necessary for the observer to view an image of the scene in its proper perspective. The designer must take into account the necessary requisites for comfortable viewing of a scene such as brightness level, contrast, magnification and resolution. Brightness to the viewer is a function of the emitted brightness of the LED,



Tolerances
.xx = ±.02
.xxx = ±.010

Figure 3-1. LED Assembly Drawing

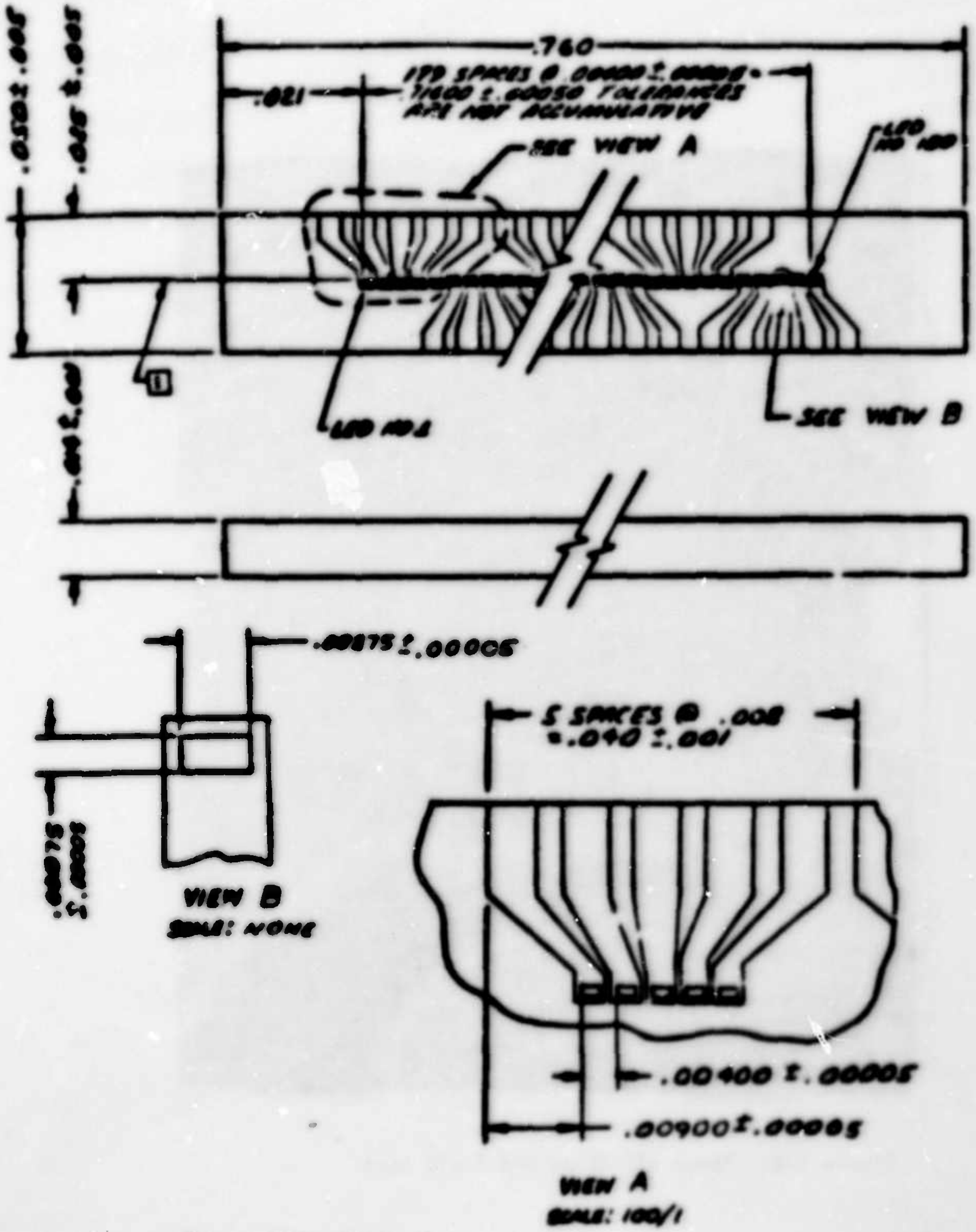


Figure 3-2. Diode Array

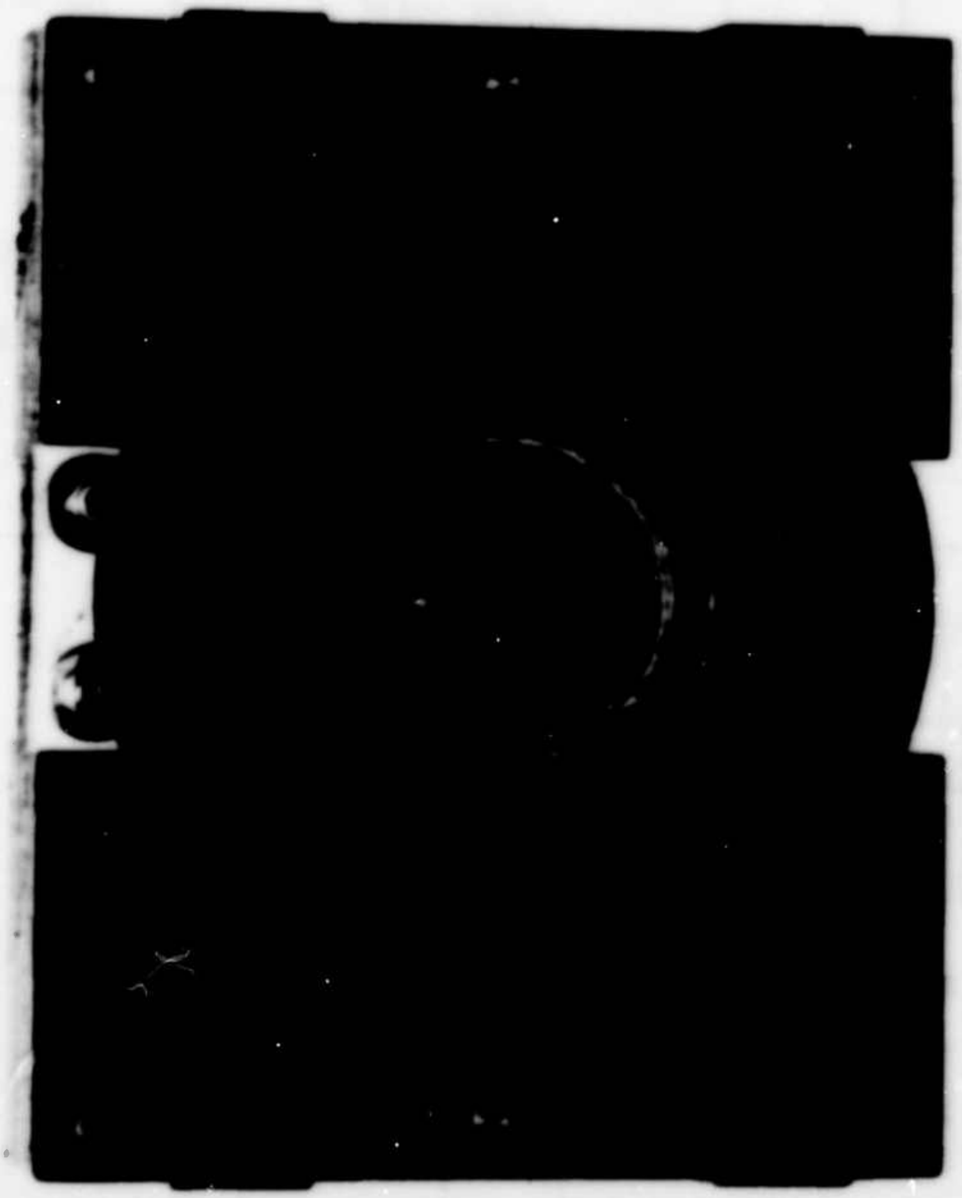


Figure 3-3. Photo LED Array and Field Lens

the F# of the visual collimator, the brightness gain of the image intensifier, and the magnification of the eyepiece lens.

The power out of the light emitting diode is proportional to the current injected into the diode. The radiant output of the diode is given as 0.94×10^{-6} watts/ma.

The maximum output is 15 ma x $94 \times 10^{-6} = 1.41 \times 10^{-5}$ watts. Converting watts to lumens, we make use of the photopic response curve which has a peak response of 685 lumens/watt at approximately 550 n.m. For the peak wavelength of LED at 660 n.m., the relative response is .06. The LED visual flux is

$$B = 1.41 \times 10^{-5} \text{ watts} \times 685 \text{ lumens/watt} \times .06$$
$$= 5.8 \times 10^{-4} \text{ lumens (max)}$$

To determine the illuminated brightness, we convert lumens to foot lamberts, which normalizes the diode into a 1 ft^2 target. For this calculation, the size of the diode is .00075 '' x .00375''

$$B = \frac{5.8 \text{ lumens} \times 144 \text{in}^2 \times 10^{-4}}{(.00075) \times (.00375) \text{ in}^2}$$
$$= 29{,}700 \text{ foot lamberts}$$

The above value must be diluted in terms of the number of scan resolution elements in the azimuth direction. The focal length of the collimator is 2.669'' and the physical angle that the scanner traverses is 6.75° yielding a 13.5° (.24 rad) optical angle. The linear excursion of the focused ray bundle of the collimator is 2.669 x .24 = .64''. The number of azimuth elements is $N = \frac{.64''}{.00075} = 853$.

$$B_v = \frac{B}{\pi} \times \frac{1}{4F_c^2} \times \frac{1}{N} \times \frac{1}{2} \times \frac{M_c^2}{M_{vc}^2}$$

The collimator F No. is $F_c = \frac{2.669}{1.58} = 1.68$

The factor of 1/2 is an interlace factor. M_c is the magnification ratio between the collimator and the afocal system and M_s is the overall system magnification. M_c is the ratio of the entrance pupil of the system narrow field to the clear aperture of the collimator.

$$M_c = \frac{63}{1.58} = 3.98$$

$$B_v = \frac{29,700}{\pi} \times \frac{1}{4(1.68)^2} \times \frac{1}{853} \times \frac{1}{2} \times \frac{(3.98)^2}{(9.8)^2}$$

$$B_v = 8.0 \times 10^{-2} \text{ lambert}$$

The image intensifier provides a brightness magnification of 60. The maximum brightness of LED display to the viewer is

$$B_v = 4.867 \text{ foot lamberts}$$

3.4 THERMAL DESIGN CONSIDERATIONS

The LED Array dissipates an average of about 0.013 watt per element. Its power dissipation depends on the number of elements used in the system and the brightness to which the individual elements are driven. Even with a large number of elements in the system, the total dissipation is so low that the LED Array can often rely on conduction through its mounting surfaces, plus convection to transfer heat to the system housing. However, in the overall system thermal design it may be desirable to provide a conductive path to a heat exchanger to reduce the general internal temperature in the system housing. Refer to Chapter 1, Section III for a discussion of the system thermal design considerations.

3.5 ELECTRICAL INTERFACE DATA

3.4.1 INPUT CHARACTERISTICS

(a) Forward voltage: 2.5 volts maximum at 15 milliamperes

(b) Current: $\geq$ 15 milliamperes per diode

3.4.2 OUTPUT CHARACTERISTICS

(a) Power: output 0.94 microwatt/milliampere minimum in the 2 to 15 milliampere range

(b) LED wavelength: wavelength of light from each LED is 6600 +50, -100 Angstrom units (A°) with all LED's normalized and biased at 4.0 volts

3.4.3 PROCESSING CHARACTERISTICS

(a) Time constant: 0.3 microsecond maximum

(b) LED array normalization parameters: resistors were selected to normalize LED light outputs to within ±5% of array average at 4.0 volts bias.

(c) Tracking: after normalization, brightness (light output) of all diodes will track within ±10% of array average brightness between bias levels of 2.5 and 8.4 volts between temperatures of 0° to +55°C as follows:

(d) Unacceptable diodes: defective diodes are those which are intermittent, shorted, crosswired with respect to connector, or fail to meet functional requirements; diodes in the array will show no defects other than shape and spacing.

(e) Shape defects: There will be no shape defects in the center 120 LED's and no more than 4 defects outside the center 120; shape defects are defined as:

(1) ≥ 15% internal area missing (< 15% internal area missing not considered a defect so long as missing area does not effect element length).

(2) missing internal area effecting diode length > 5% (missing internal area effecting diode length ≤ 5% is not considered a defect).

(3) ≥ 5% additional external area (< 5% additional external area is not considered a defect).

SECTION IV

ALIGNMENT/MAINTENANCE

4.1 GENERAL

This section provides information on the test and alignment requirements to be considered in the use and application of the LED Array.

4.2 MAINTENANCE

The LED array is not considered field repairable. Corrective maintenance consists of failed unit replacement only. The test and inspection procedures outlined in this section may be used to determine inoperative modules.

4.3 EQUIPMENT FOR TESTING

Standard test equipment such as ohmmeters, VTVMs or digital voltmeters cannot be safely used to check the LED array.

4.4 SPECIAL TEST EQUIPMENT

The following special test equipment required to complete the test provided in this section is a LED array module test set. This test set must be fabricated. Refer to Figure 4-1 and fabricate test from the supplied schematic.

Using the test set apply the probe tips to the pins described in Figure 4-1, while an assistant views the LED array output in subdued lighting. If illumination is obtained from each of the diode elements, the array is functionally acceptable.

4.5 ALIGNMENT

When the LED is assembled to the collimator, an alignment and focus check must be made. The number of degrees of freedom requiring check out are enumerated

- Longitudinal or axial which results in defocus

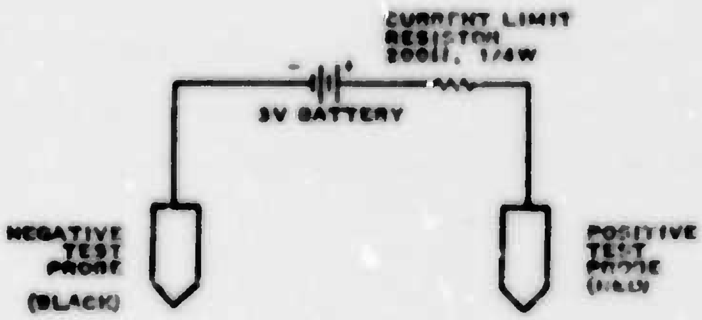


Figure 4-1. Test Set Up

- Transverse left/right (azimuth
  up/down (elevation)

- Rotational - results in picture tilt if the array is not vertical to the scan direction.

The LED array is the last module in the overall assembly to be aligned. Thus, aligning the module assures that the scanner, IR imager and detector and visual collimator has already been properly aligned. Also for this test, the visual display optics should not be used. The common module unit should be mounted on an optical bench and an optical boresighting scope with sufficient magnification (10 x or higher) should be used to focus and align the LED array. The common module unit is down powered and the scan mirror must be accurately locked to a 45° center position. At least three elements of the LED need be illuminated for this test; the two extreme end elements and a center element. These elements can be illuminated using a device similar to the LED array test set.

APPENDIX I

The Effect of Atmosphere on Energy Transmission

Consider two display elements of equal size one containing a target and the other containing only background. In the absence of atmosphere the signal from the target element will be I_S, that from background will be I_B .

The parameter of interest is the difference in signal

$$I_S - I_B$$

In the presence of atmospheric scattering and absorption I_S and I_B become

for the IR

$$I_{S_{atm}} = I_S\, e^{-(\alpha_s + \alpha_a)x} + I_B\,(1 - e^{-\alpha_s x})\, e^{-\alpha_a x} + I_B\,(1 - e^{-\alpha_a x})$$

$$I_{B_{atm}} = I_B$$

for the visible

$$I_{S_{atm}} = I_S\, e^{-(\alpha_s + \alpha_a)x} + I_B\,(1 - e^{-\alpha_s x})\, e^{-\alpha_a x}$$

$$I_{B_{atm}} = I_B\, e^{-\alpha_a x}$$

where α_s = scattering coefficient

α_a = absorption coefficient

x = range to target

and

$I_S\, e^{-(\alpha_s + \alpha_a)x}$	:	the signal reduced by atmospheric scattering and absorption
$I_B\,(1-e^{-\alpha_s x})e^{-\alpha_a x}$	:	$I_B(1-e^{-\alpha_s x})$ is the amount of background energy scattered into the signal element. This energy is attenuated by approximately $e^{-\alpha_a x}$
$I_B\,(1-e^{-\alpha_a x})$	:	The amount of energy radiated by the column of atmosphere between the target and sensor. The atmosphere is assumed to be at the same temperature as the background. This component, of course, does not exist for the visible.

The $I_{B_{atm}}$ is found by setting $I_S = I_B$ in the expression for $I_{S_{atm}}$

Therefore, the differential signal is

IR $\quad I_{S_{atm}} - I_{B_{atm}} = (I_S - I_B)e^{-(\alpha_a + \alpha_s)x}$

Visible $\quad I_{S_{atm}} - I_{B_{atm}} = (I_S - I_B)e^{-(\alpha_a + \alpha_s)x}$

APPENDIX II

ULTIMATE PERFORMANCE OF AN ELEMENTAL DETECTOR VIEWING A BAR PATTERN(U)

Assume a target with aspect ratio of 2:1 and angular dimensions 2σ by σ. This aspect ratio is characteristic of many targets (e.g., trucks, tanks, men) that one might encounter in the field. The Johnson criterion states that the probability of perception of this target is exactly equal to that of an equivalent bar pattern of 4 cycles/minimum dimension

Calculating the S/N in a single bar.

The video signal in an ideal device (unit quantum efficiency, photon noise limited) is:

$$S = (Q_s - Q_B)\frac{A_d}{f^2} A_c \tau \qquad (1)$$

where:

Q_s = flux from a resolution element containing signal (photon/sec cm^2-ster)

Q_B = flux from a resolution element containing background (photon/sec-cm^2 - ster)

A_D = area of detector element (cm^2)

A_C = area of collecting optics (cm^2)

f = optics focal length (cm)

τ = dwell time of element on a point in the scene (sec)

$\frac{A_D}{f^2}$ = solid instantaneous field of a detector (ster)

The noise is the uncertainty in the signal element

$$N = \left(Q_s \frac{A_D}{f^2} A_C \tau\right)^{1/2} \qquad (2)$$

From Eq1 and Eq2 the video S/N

$$S/N = \frac{Q_s - Q_B}{Q_s^{1/2}}\left(\frac{A_d}{f^2} A_c \tau\right)^{1/2} \overset{\sqcap}{\text{MTF}}\,(f_r) \qquad (3)$$

Since the image is a periodic bar pattern of spatial frequency, fr, the S/N must be modified by the square wave transfer function of the system, corresponding to that spatial frequency $\widetilde{MTF}$ (fr)

The display $\frac{S}{N}$, that perceived by the eye, may be improved over the video S/N by temporal and spatial integration of the eye,

$$\frac{S}{N} = \frac{Q_s - Q_B}{Q_s^{1/2}} \left(\frac{A_D}{f^2} A_C \tau \right)^{1/2} \widetilde{MTF}_{(fr)} \left(\frac{t_e}{T_F} \right)^{1/2} n^{\frac{1}{2}} \qquad (4)$$

where:

$\frac{t_e}{T_F} = \frac{\text{eye integration time}}{\text{frame time}}$ = number of frames available for integration

n = number of resolution elements on a single bar of the pattern

The improvement goes as the 1/2 power because the signal is non-randomly generated and will build linearly the number of samples integrated, whereas the noise is randomly generated and tends to build only as the 1/2 power.

Rearranging terms,

$$\frac{S}{N} = \frac{Q_s - Q_B}{Q_s^{1/2}} \left(\frac{t_e A_D}{f^2} A_C \right)^{1/2} \left| \frac{\tau}{T_F} \right|^{1/2} n^{1/2} \widetilde{MTF}_{optics}(fr) \widetilde{MTF}_{detector}(fr) \qquad (5)$$

BUT

$$\frac{\tau}{T_F} = \left(\frac{1}{\text{number of scene elements}} \right) = \frac{A_D/f^2}{FOV^2} \qquad (6)$$

$$n = \frac{(\sigma/2n_r)2\sigma}{A_D/f^2} = \frac{\sigma^2}{N_r A_D/f^2} \qquad (7)$$

The $\widetilde{MTF}$ is related to the sine wave MTF by

$$\widetilde{MTF}\,(fr) = \frac{4}{\pi}\left[MTF\,(f_r) - 1/3\ MTF\,(3fr) + 1/5\ MTF\,(5fr) - \cdots\right] \quad (8)$$

Assume for the present, that the spatial frequency of the bar pattern is greater than one third the cut-off frequency of the detector so that

$$\widetilde{MTF} = \frac{4}{\pi}\ MTF \quad (9)$$

The MTF of a scanning detector is

$$\frac{\sin \pi f_r \sqrt{\frac{A_D}{f^2}}}{\pi f_r \sqrt{\frac{A_D}{f^2}}} \quad (10)$$

Combining terms and inserting Eqs 9 and 10 in Eq 5

$$\frac{S}{N} = \frac{Q_s - Q_B}{Q_s^{1/2}}\ (.2\ Ac)^{1/2}\ \frac{1}{FOV}\ \frac{\sigma}{n_r^{1/2}}\ \frac{4}{\pi}\ \frac{\sin\left(\pi fr \sqrt{\frac{A_D}{f^2}}\right)}{\pi\ fr}\ \widetilde{MTF}_{optics} \quad (11)$$

BUT:

$$fr = \frac{n_r}{\sigma}$$

SO:

$$\frac{S}{N} = \frac{Q_s - Q_B}{Q_s^{1/2}}\ (.2Ac)^{1/2}\ \frac{1}{FOV}\ \frac{\sigma^2}{n_r^{3/2}}\ 4\ \frac{\sin\left(\pi \frac{n_r}{\sigma} \sqrt{\frac{A_D}{f^2}}\right)}{\pi^2}\ MTF_{optics} \quad (12)$$

The optimum detector size $\sqrt{\frac{A_D}{f^2}}$ when

$$\frac{d(S/N)}{d\sqrt{\frac{A_D}{f^2}}} = 0$$

This occurs when $\frac{\pi n_r}{\sigma}\sqrt{\frac{A_D}{f^2}} = \frac{\pi}{2}$

AD-A118 049 MAGNAVOX GOVERNMENT AND INDUSTRIAL ELECTRONICS CO MA--ETC F/G 9/5
PRELIMINARY COMMON MODULE DESIGN HANDBOOK.(U)
APR 76 DAAG53-75-C-0178
UNCLASSIFIED GSDR-900 NL

5 OF 5
AD
A118049

END
DATE
FILMED
9-82
DTIC

SO:

$$\sqrt{\frac{A_D}{f^2}} = \frac{\sigma}{2n_r}$$

This is just the width of a single bar. The assumption of Eq 9 that the spatial frequency of the bar, n_r/σ, is greater than f cut-off/3 is valid since f cut-off of a detector with IFOV $= \sqrt{\frac{A_D}{f^2}} = \frac{\sigma}{2n_r}$ is $\frac{1}{\text{IFOV}} = \frac{2n_r}{\sigma}$

Eq 12 may be expressed in terms of a minimum resolvable temperature, T, once a threshold S/N is specified

$$\Delta T = \frac{S}{N}\, Q_s^{1/2} \left(\frac{\text{FOV}}{(.2\, A_C)}\right)^{1/2} \frac{n_r^{3/2}}{\sigma^2} \left(\frac{\pi}{4}\right)^2 \frac{1}{\text{MTF}_{\text{optics}}} \Big/ \frac{dQ}{dT}$$

ME

8